OMRON USER'S MANUAL

Programmable Controller

Model SYSMAC-**P5R**

ONICS CO.

INTRODUCTION

"OMRON SYSMAC" is the trade name of OMRON's programmable controllers unparalleled in reliability and versatility.
Programmable controllers, which were initially developed to meet the demands by equipment manufacturing industries and large-scale plants for their production facilities, now answer the needs of industries from every field and have become original equipment for installation at factories.
The above trend has induced original equipment manufacturers to design the incorporation of programmable controllers in their machinery and equipment, and thus the demand for availability of the programmable controllers that can be handled as easily as components has been increasing. Accordingly, OMRON has sought to develop programmable controllers which are: a. small and economical, b. easy to handle by merely connecting a load and power, and c. easy to operate by anyone at site, in addition to possessing flexibility that permits adapting to changes to the controlled systems or control parameters with simple keyboard operation and high reliability which can be materialized only by electronic control.
OMRON now offers with confidence the OMRON SYSMAC-P5R Package Type Programmable Controller, a first-class programmable controller with "CPU function" and "techniques responding adequately to the needs at every site." Programming with the SYSMAC-P5R can be performed easily and directly from ladder diagrams and/or timing charts using the program console incorporated in the programmable controller. Two sister products are also available for your choice; Model SYSMAC-P0 Step Advance Type Sequence Controller which employs the timing chart programming method and Model SYSMAC-P0R Package Type Programmable Controller which employs the ladder diagram programming method.

CONTENTS

1. Features

- **Flexible programming**
  With a variety of functions fully packaged in a single enclosure, the SYSMAC-P5R permits the combined use of ladder diagram and timing chart (step advance type) programming methods, in addition to the choice of using either of the two methods.
- **Integrated program console**
  The central processing unit (CPU) incorporates a program console which is provided with an abundance of operational check functions in addition to programming.
- **Continuity checking is possible according to the sequence of ladder diagram**
  The SYSMAC-P5R is capable of retrieving an instruction word (output instruction) during the program execution to check the circuit block concerned for electrical continuity according to the sequence of the ladder diagram. Furthermore, it monitors the present value of each timer or counter, thus facilitating the program simulation and maintenance operations of the controller.
- **A maximum of four program patterns can be written into the EPROM in units of 2k words per pattern.**
  After the program writing, a user program can be selected for execution by operating the program console.
- **Built-in PROM writer function**
  Permits writing of a debugged program into the EPROM.
- **Programs can be recorded on cassette tape**
  By connection of the exclusive interface cords, programs in the CPU memory may be dumped onto a commercially available cassette tape.
- **Set value of timer/counter can be changed while the controller is in operation**
- **Built-in 24-hour clock**
  With the 24-hour clock incorporated in the CPU, time of day control can be programmed freely.
- **3 parallel operations are possible by the step advance type programming.**
- **Electronic buzzer alarms**
  Two kinds of alarms are issued to alert the operator upon detection of a program error, key input error, or circuit error, thus facilitating programming and simulation.

2. System Configuration and Specifications

2.1 Available Types

The SYSMAC-P5R consists of a central processing unit (CPU) and an I/O unit. A PROM writer and a cassette interface are contained in the CPU.

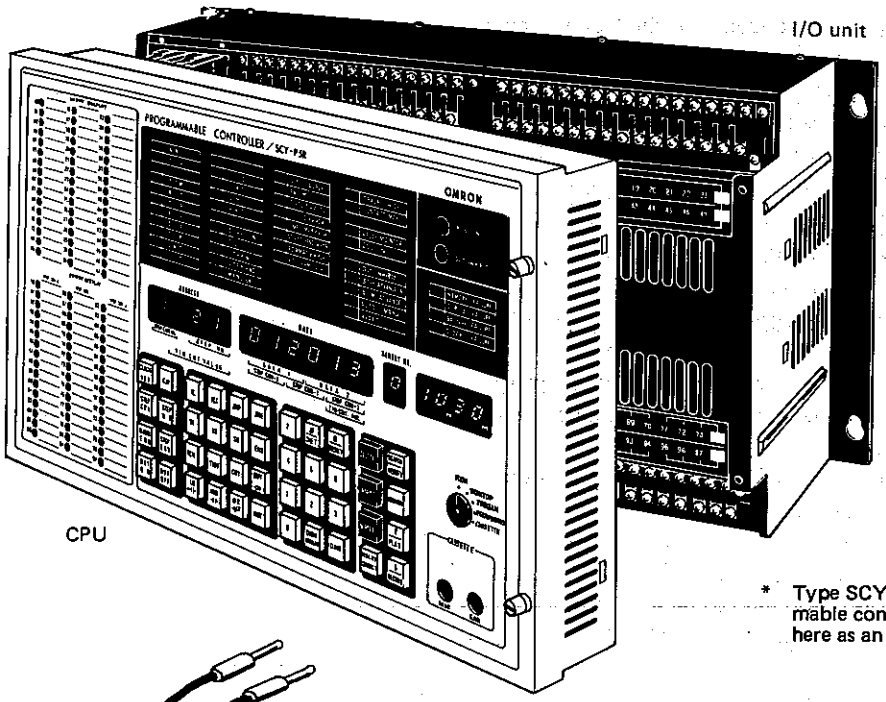
■ PROGRAMMABLE CONTROLLER

Classification	Specification	No. of I/O points	Type
RAM & ROM type	RAM & ROM type CPU, Cassette I/F, PROM writer, 24-hour clock	48 input points 48 output points	SCY-P5R10E
		32 input points 24 output points	SCY-P5R30E

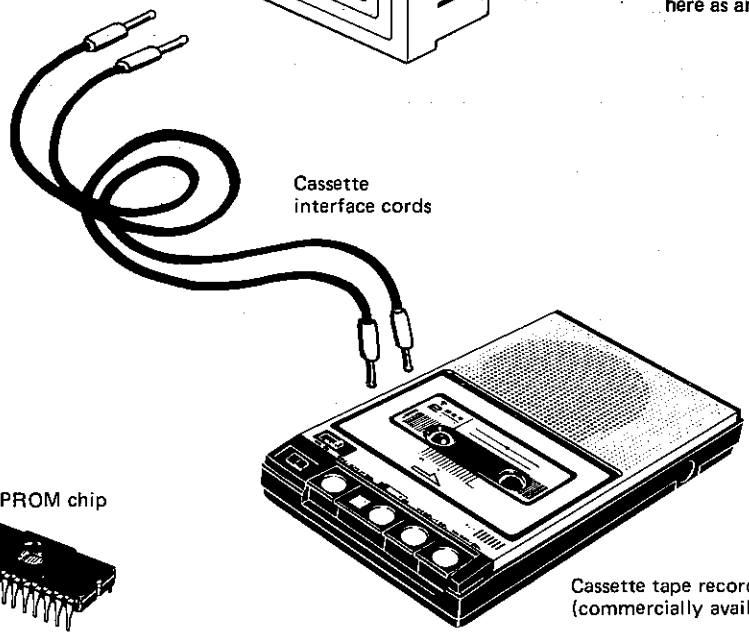
■ ACCESSORIES

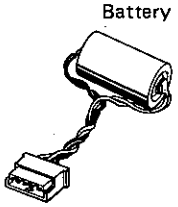
Classification	Specification	Type
Cassette interface cord	For connection between CPU and cassette tape recorder Weight: Approx. 50g	SCYP0R-PLG01
EPROM chip	Weight: Approx. 10g	ROM-2732
Battery	3V lithium battery with connector Weight: Approx. 20g	SCYP5R-BAT01

NOTE: * OMRON offers Type ROM-2732 (equivalent to 2732) developed under strict quality control as the EPROM (2k) chip for OMRON Programmable Controller series. Be sure to use this EPROM chip for the OMRON Programmable Controllers.



* Type SCY-P5R10E programmable controller is shown here as an example.

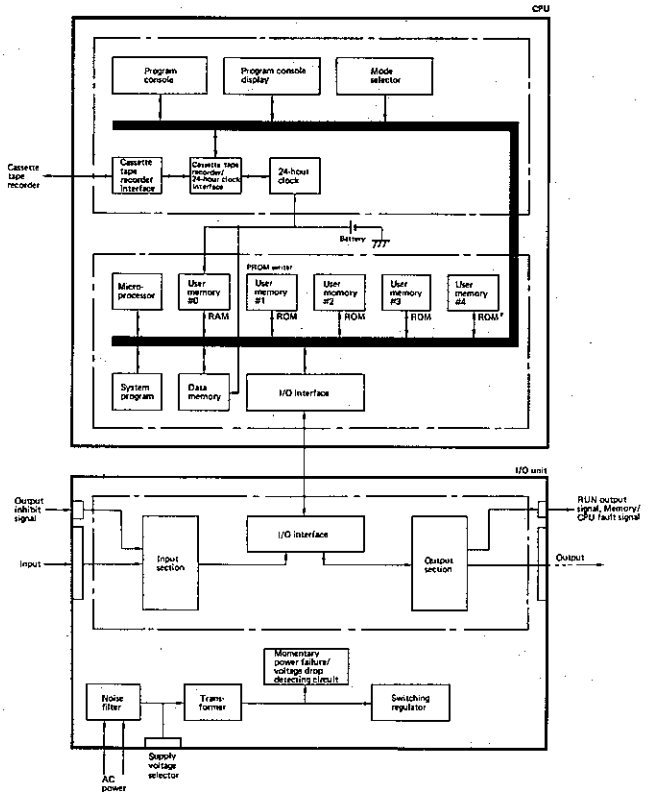



Battery

EPROM chip

2.2 System Configuration

The system block diagram of the Type SCY-P5R10E/ SCY-P5R30E (RAM & ROM type) is shown below.



2.3 Specifications

■ RATINGS

Supply voltage	AC 110, 120, 220 or 240V, 50/60Hz*
Operating voltage range	85 to 110% of rated voltage**
Power consumption	160VA max.
Insulation resistance	10MΩ min. at DC 500V (between external terminal and outer casing)
Dielectric strength	AC 1,500V, 50/60Hz for 1 minute (between external terminal and outer casing)
Noise immunity	1,000Vp-p Rise time: 1nsec; Pulse width: 2μsec
Vibration	16.7Hz, 3mm double amplitude for 2 hrs.
Shock	10G's (in X, Y, Z directions, respectively 3 times)
Ambient temperature	Operating: 0 to +50°C Storage: −10 to +70°C (without battery)
Humidity	30 to 90% RH (without condensation)
Atmosphere	Must be free from corrosive gases
Structure	Package type
Coating	CPU: Ivory white I/O unit: Dark gray
Weight	SCY-P5R10E: 15.8kg max. SCY-P5R30E: 12kg max.

NOTE: * Set the supply voltage selector switch to select the required voltage.

** A momentary power failure of less than 1/2 cycle is ignored by the programmable controller. If a momentary power failure of 1/2 to 1 cycle occurs, the power failure condition may or may not be detected by the programmable controller since it is in an unstable area. If a power failure of more than 1 cycle occurs, the programmable controller detects the power failure.

■ CHARACTERISTICS

Control system	Stored program system
Main control element	LSI, TTL, C-MOS
Programming system	Ladder diagram and/or timing chart (step advance type) programming
Instruction word length	1 word, 2 words, 4 words, 7 words
Number of instructions	24 kinds
Scan time	Ladder diagram type: 38msec/1k words Step advance type: 500μsec/step controller + 9msec
Programming capacity	Ladder diagram type SCY-P5R10E: RAM 2k words EPROM 2k words x 4 banks SCY-P5R30E: RAM 1k words EPROM 1k words x 4 banks Step advance type* SCY-P5R10E: RAM 99 steps x 3 step controllers EPROM 99 steps x 3 step controllers x 4 banks SCY-P5R30E: RAM 99 steps x 2 step controllers EPROM 99 steps x 2 step controllers x 4 banks
Number of input points	SCY-P5R10E 48 points (Relay Nos. 000 ~ 047) SCY-P5R30E 32 points (Relay Nos. 000 ~ 031)
Number of output points	SCY-P5R10E 48 points (Relay Nos. 050 ~ 097) SCY-P5R30E 24 points (Relay Nos. 050 ~ 073)
Number of internal auxiliary relays	SCY-P5R10E 152 points (Relay Nos. 098 ~ 249) SCY-P5R30E 176 points (Relay Nos. 074 ~ 249)
Number of special auxiliary relays	6 points (Relay Nos. 250 ~ 255) • 250: 0.1sec clock • 251: 1sec clock • 252: 1 min clock • 253: Turns ON when the battery is abnormal. • 254: Turns ON when the 24-hour clock is abnormal. • 255: Normally ON
Number of latching relays	64 points (Relay Nos. 00 ~ 63)
Number of shift registers	64 points (Relay Nos. 00 ~ 63) 8 bits x 8 points
Number of temporary memory relays	8 points (Relay Nos. 0 ~ 7)
Number of timers and counters	Ladder diagram type: 64 points (Relay Nos. 00 ~ 63) Timer: 0.1 ~ 99.9sec Counter: 1 ~ 999 counts Step advance type: Timer: 0.1 ~ 25.5sec 1 ~ 255sec 1 ~ 255 min Counter: 1 ~ 255 counts
Timer accuracy	±(Set value x 1% + 0.1sec)
Counter response speed	10Hz max./1k words
24-hour clock accuracy	±1 min per month
Memory protective function against power failure	Ladder diagram type: Status data of respective latching relays, counters and shift register before the power failure are retained in the memory. Step advance type: Status data of step No. before the power failure are retained in the memory.
Diagnostic functions	Memory failure (Parity check) CPU failure (Watchdog timer) Battery failure (Battery not loaded, battery voltage drop) Clock failure (24-hour clock stops) Program check • Coil duplication check • END instruction check • Circuit error check (syntax check) • IL-ILC error • JMP-JME error • STEP-STEP END error • Format error • Program over

NOTES: * With the step advance type instructions, up to 99 steps can be programmed per step controller. However, note that the number of program steps cannot exceed the programming capacity of 2k words when all the 3 step controllers are used.

■ INPUT

Input form	No-voltage contact input (photocoupler isolation)
Input voltage	DC 20V (built-in power supply)
Input current	10mA
Input operation level	ON: 5mA min. OFF: 2mA max.
Input response speed	10Hz max.
Input impedance	1.8kΩ
Input terminal configuration	8 points/common (terminal block connector)
Operation indication	LED's on the front panel of the CPU (The corresponding LED illuminates when the input is ON.)

■ OUTPUT

Output form	Relay (SPST-NO) contact output (no-voltage)
Output relay	SCY-P5R10E Output relay Nos. 050 ~ 097 OMRON Type MY2* SCY-P5R30E Output relay Nos. 050 ~ 069 OMRON Type G2L Output relay Nos. 070 ~ 073 OMRON Type MY2*
Maximum applicable load	DC 30V/AC 250V 2A, resistive load DC 30V/AC 250V 0.8A, inductive load
Output terminal configuration	3 points/common (terminal block connector)**
Operation indication	LED's on the front panel of the CPU (The corresponding LED illuminates when the output is ON.)

NOTES: * Interchangeable with OMRON Model G3F solid-state relay.
** 4A max. per common terminal.

■ DIAGNOSTIC FUNCTIONS

As the diagnostic functions of the SYSMAC-P5R, checks on the items listed in the following tables are performed in the PROGRAM and RUN (MONITOR) modes, respectively.

• PROGRAM mode

Diagnostic function		Function	Error indication
Item	Title		
Program check	Coil duplication check	Checks coil numbers for duplication.	ON
	END instruction check	Checks the presence of END instruction at the end of the program.	ON
	Circuit error check	Checks the circuit for proper configuration.	ON
	IL-ILC error check	Checks if IL and ILC instructions are being used in pairs.	ON
	JMP-JME error check	Checks if JMP and JME instructions are being used in pairs.	ON
	STEP-STEP END error check	Checks if STEP. CON and STEP. END or MANU. END instructions are being used in pairs.	ON
	Format error check	Checks each instruction for proper format.	ON
	Program over check	Checks if the number of program steps exceeds the memory capacity in Insert or Write operation.	ON

NOTE: In the "Program Over" condition, entries by the Insert or Write key will be ignored.

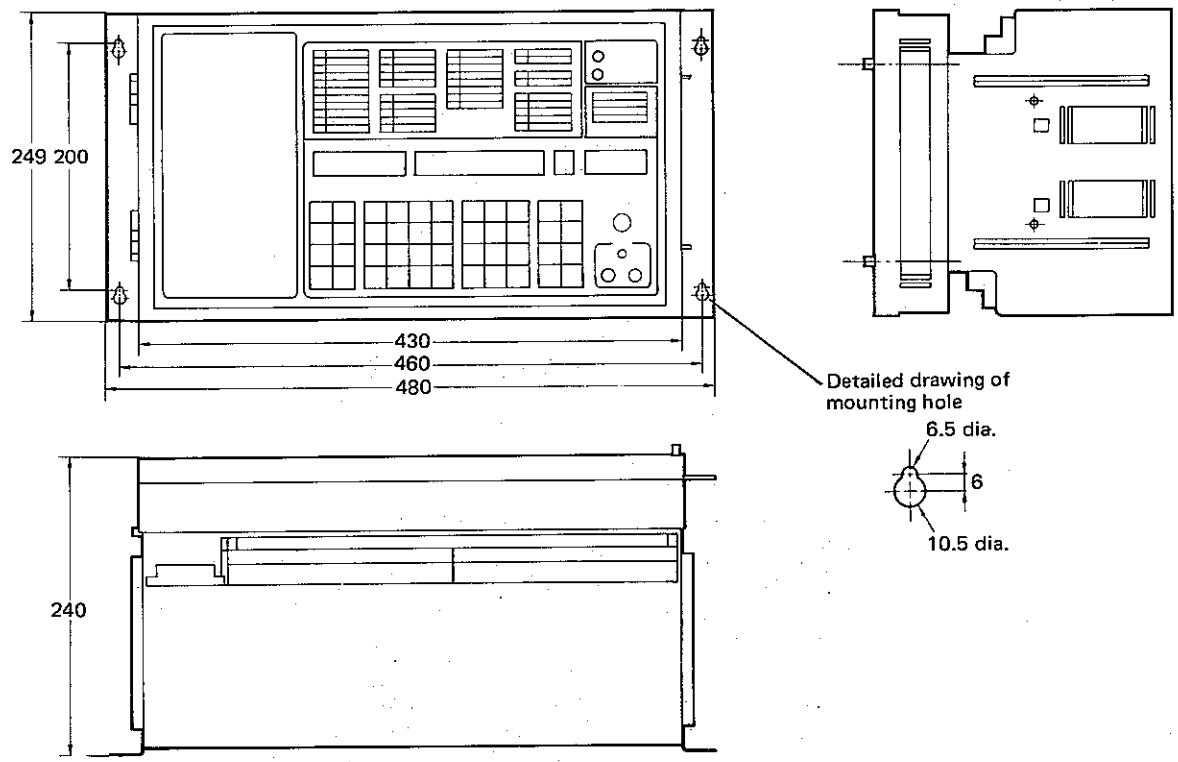
• RUN (MONITOR) mode

Diagnostic function		Indication				Control I/O relay contacts****		Special internal auxiliary relay
Item	Title	ADDRESS display	DATA display	RUN indicator	FAULT indicator	RUN output	Memory/CPU failure output	
Memory failure	Parity check	Address where a parity error has occurred.	Parity error data*	OFF	ON	Open	Closed	–
CPU failure	Watchdog timer check	OFF	OFF	OFF	ON	Open	Closed	–
Battery failure**	Rated voltage check, Battery loading check	–	–	ON	ON	Closed	Open	253: ON
24-hour clock failure***	Clock operation check	–	–	ON	ON	Closed	Open	254: ON

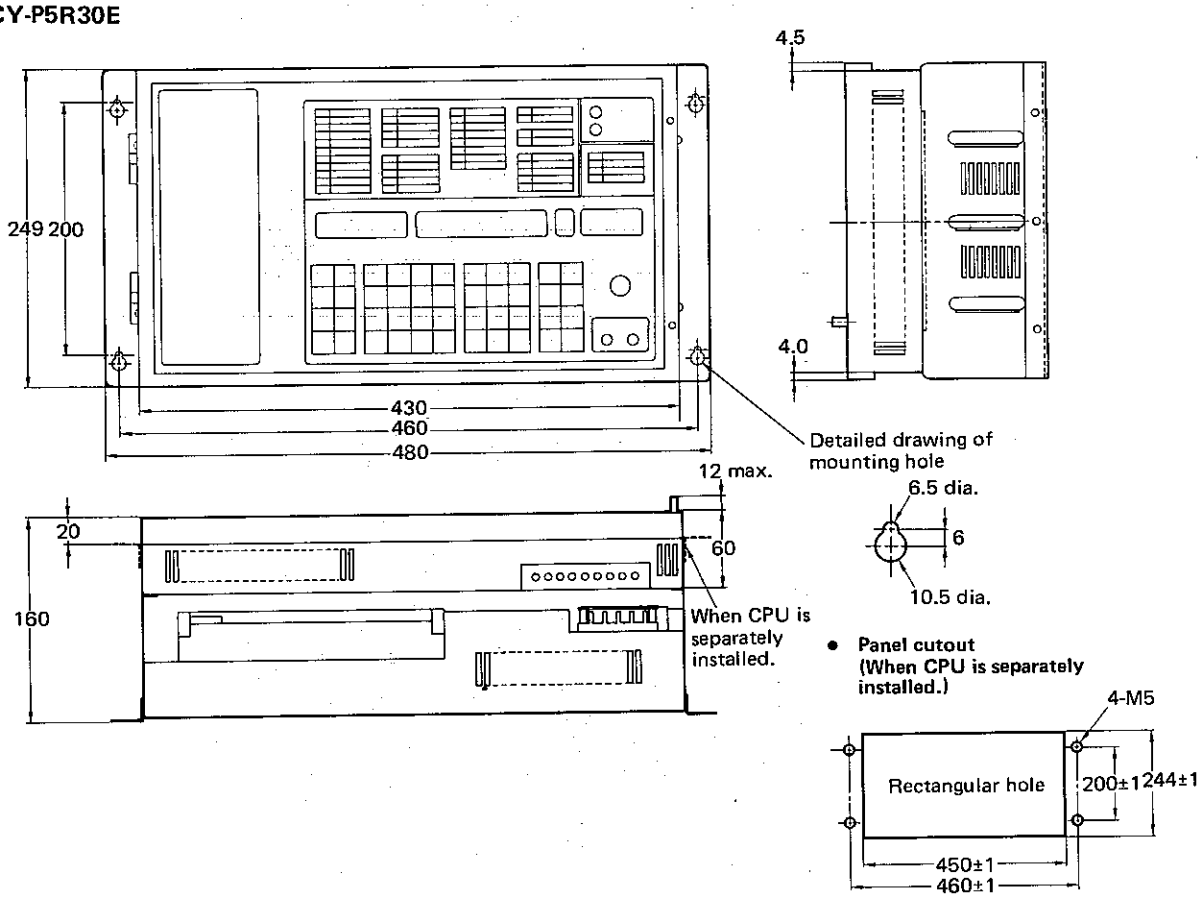
NOTES: * When only the parity bit is destroyed, data is displayed properly.
** The lithium battery checks are performed in all the modes. After the BATTERY FAILURE indicator illuminates, be sure to replace the battery within a week, or the contents of the program memory will be destroyed.
*** The CLOCK FAILURE indicator illuminates when the 24-hour clock is stopped or the time is advanced (in the MONITOR mode), but this condition may be cleared by depressing the CLEAR key.
**** Refer to Section 6.6 for the use of the Control I/O Relay.

2.4 Dimensions

■ Type SCY-P5R10E



■ Type SCY-P5R30E

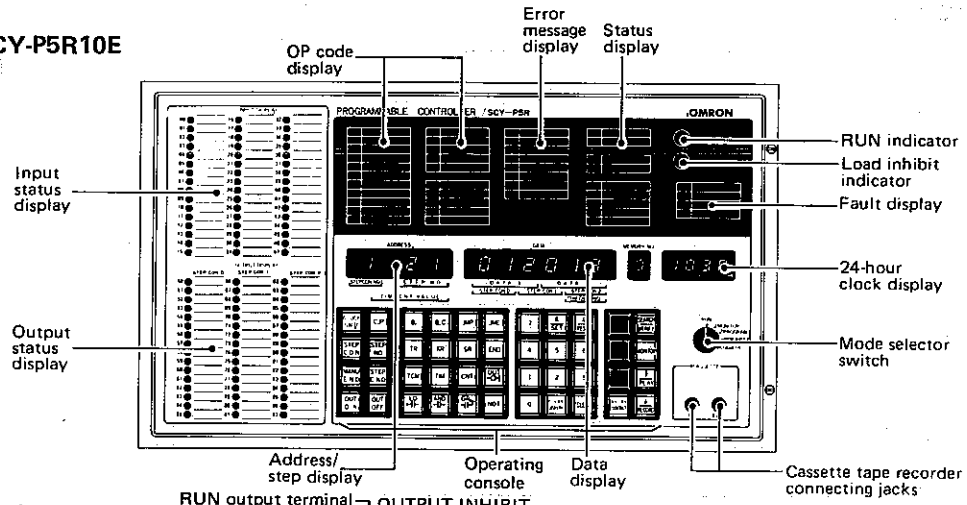


- **Panel cutout (When CPU is separately installed.)**

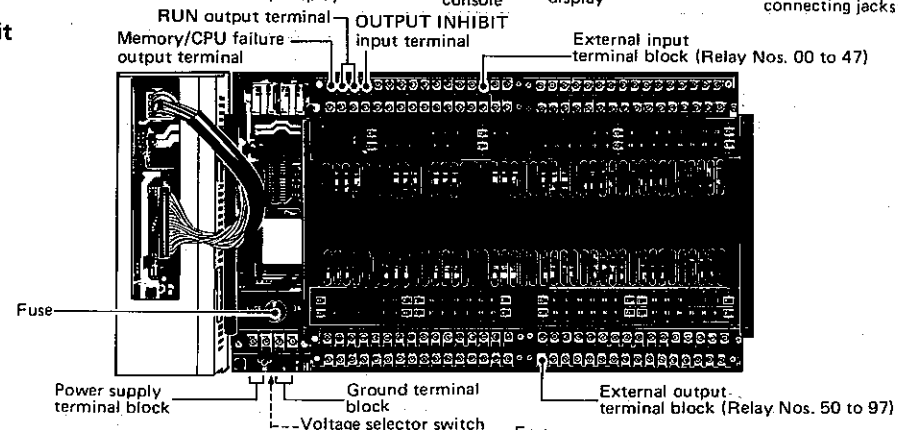
2.5 Names of Respective Parts

■ Type SCY-P5R10E

• CPU

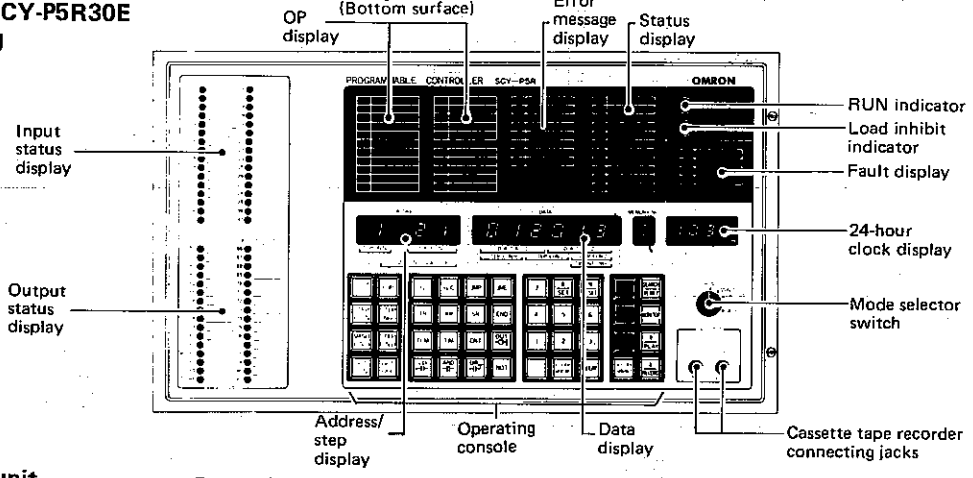


• I/O unit

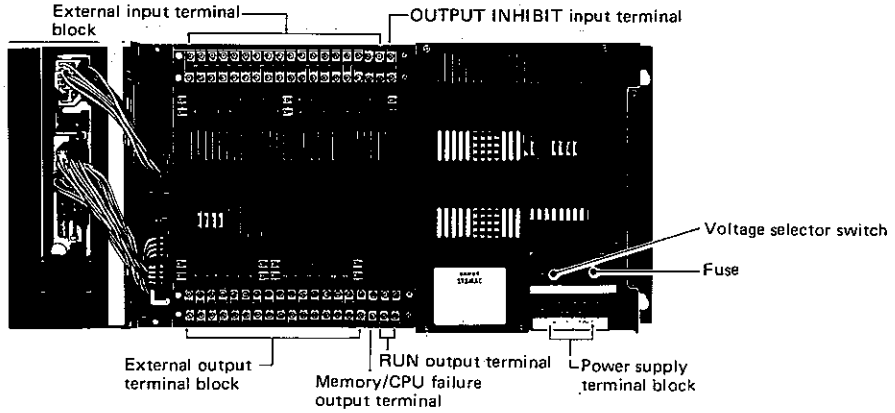


■ Type SCY-P5R30E

• CPU



• I/O unit



3. Ladder Diagram Programming

3.1 Assignment of Relay Numbers

Relay numbers correspond to the data memory areas and the operation (ON/OFF state) of each relay is stored in the corresponding memory area.

The method of assigning relay numbers used for the ladder diagram programming is as follows.

3.1.1 List of relay numbers

- **Type SCY-P5R10E**

Name	No. of points	Symbol	Relay number									
Input relay	48	—	000	001	002	003	004	005	006	007	008	009
			010	011	012	013	014	015	016	017	018	019
			020	021	022	023	024	025	026	027	028	029
			030	031	032	033	034	035	036	037	038	039
			040	041	042	043	044	045	046	047		
Output relay	48	—	050	051	052	053	054	055	056	057	058	059
			060	061	062	063	064	065	066	067	068	069
			070	071	072	073	074	075	076	077	078	079
			080	081	082	083	084	085	086	087	088	089
			090	091	092	093	094	095	096	097		
Internal auxiliary relay	152	—									098	099
			100	101	102	103	104	105	106	107	108	109
			110	111	112	113	114	115	116	117	118	119
			120	121	122	123	124	125	126	127	128	129
			130	131	132	133	134	135	136	137	138	139
			140	141	142	143	144	145	146	147	148	149
			150	151	152	153	154	155	156	157	158	159
			160	161	162	163	164	165	166	167	168	169
			170	171	172	173	174	175	176	177	178	179
			180	181	182	183	184	185	186	187	188	189
			190	191	192	193	194	195	196	197	198	199
			200	201	202	203	204	205	206	207	208	209
			210	211	212	213	214	215	216	217	218	219
			220	221	222	223	224	225	226	227	228	229
			230	231	232	233	234	235	236	237	238	239
			240	241	242	243	244	245	246	247	248	249
Timer and counter	64	TIM CNT	00	01	02	03	04	05	06	07	08	09
			10	11	12	13	14	15	16	17	18	19
			20	21	22	23	24	25	26	27	28	29
			30	31	32	33	34	35	36	37	38	39
			40	41	42	43	44	45	46	47	48	49
			50	51	52	53	54	55	56	57	58	59
			60	61	62	63						
Latching relay	64	KR	00	01	02	03	04	05	06	07	08	09
			10	11	12	13	14	15	16	17	18	19
			20	21	22	23	24	25	26	27	28	29
			30	31	32	33	34	35	36	37	38	39
			40	41	42	43	44	45	46	47	48	49
			50	51	52	53	54	55	56	57	58	59
			60	61	62	63						

Name	No. of points	Symbol	Relay number							
Shift register	8 bits x 8	SR	00	01	02	03	04	05	06	07
			10	11	12	13	14	15	16	17
			20	21	22	23	24	25	26	27
			30	31	32	33	34	35	36	37
			40	41	42	43	44	45	46	47
			50	51	52	53	54	55	56	57
			60	61	62	63	64	65	66	67
			70	71	72	73	75	75	76	77
Temporary memory relay	8	TR	0	1	2	3	4	5	6	7

NOTE: For the ladder diagram programming with the SCY-P5R10E relay numbers other than above cannot be used.

Name	No. of points	Relay number	Description
Special auxiliary relay	6	250	0.1sec clock
		251	1sec clock
		252	1min clock
		253	Turns ON when the battery is abnormal.
		254	Turns ON when the 24-hour clock is abnormal.
		255	Normally ON

- **SCY-P5R30E**

Name	No. of points	Symbol	Relay number									
Input relay	32	—	000	001	002	003	004	005	006	007	008	009
			010	011	012	013	014	015	016	017	018	019
			020	021	022	023	024	025	026	027	028	029
			030	031								
Output relay	24	—	050	051	052	053	054	055	056	057	058	059
			060	061	062	063	064	065	066	067	068	069
			070	071	072	073						
Internal auxiliary relay	176	—					074	075	076	077	078	079
			080	081	082	083	084	085	086	087	088	089
			090	091	092	093	094	095	096	097	098	099
			100	101	102	103	104	105	106	107	108	109
			110	111	112	113	114	115	116	117	118	119
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			150	151	152	153	154	155	156	157	158	159
			160	161	162	163	164	165	166	167	168	169
			170	171	172	173	174	175	176	177	178	179
			180	181	182	183	184	185	186	187	188	189
			190	191	192	193	194	195	196	197	198	199
			200	201	202	203	204	205	206	207	208	209
			210	211	212	213	214	215	216	217	218	219
			220	221	222	223	224	225	226	227	228	229
			230	231	232	233	235	235	236	237	238	239
			240	241	242	243	244	245	246	247	248	249
Timer and counter	64	TIM CNT	00	01	02	03	04	05	06	07	08	09
			10	11	12	13	14	15	16	17	18	19
			20	21	22	23	24	25	26	27	28	29
			30	31	32	33	34	35	36	37	38	39
			40	41	42	43	44	45	46	47	48	49
			50	51	52	53	54	55	56	57	58	59
			60	61	62	63						
Latching relay	64	KR	00	01	02	03	04	05	06	07	08	09
			10	11	12	13	14	15	16	17	18	19
			20	21	22	23	24	25	26	27	28	29
			30	31	32	33	34	35	36	37	38	39
			40	41	42	43	44	45	46	47	48	49
			50	51	52	53	54	55	56	57	58	59
			60	61	62	63						

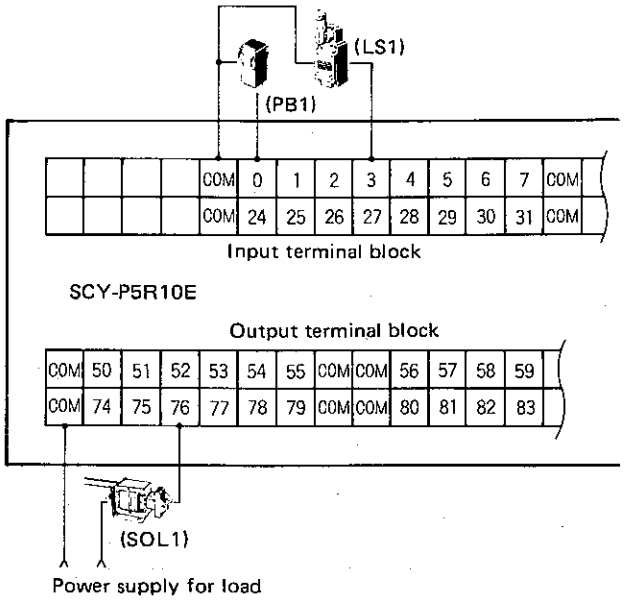
Name	No. of points	Symbol	Relay number							
Shift register	8 bits x 8	SR	00	01	02	03	04	05	06	07
			10	11	12	13	14	15	16	17
			20	21	22	23	24	25	26	27
			30	31	32	33	34	35	36	37
			40	41	42	43	44	45	46	47
			50	51	52	53	54	55	56	57
			60	61	62	63	64	65	66	67
			70	71	72	73	74	75	76	77
Temporary memory relay	8	TR	0	1	2	3	4	5	6	7

Name	No. of points	Relay number	Description
Special auxiliary relay	6	250	0.1sec clock
		251	1sec clock
		252	1min clock
		253	Turns ON when the battery is abnormal.
		254	Turns ON when the 24-hour clock is abnormal.
		255	Normally ON

NOTES: 1. For the ladder diagram programming with the SCY-P5R30E, relay numbers other than above cannot be used.
2. For setting the timer and counter values, values 001 thru 999 are used. The timer/counter numbers are shared by both timers and counters. Therefore, a number already assigned to a timer cannot be used for any other counter.
3. Relay numbers may not necessarily be assigned consecutively.

3.1.2 Determination of I/O relay numbers

1. In a sequence circuit diagram which is generally known, a sequence circuit is drawn with input/output devices included and I/O device symbols and relay numbers are arbitrarily determined. However, since the SYSMAC-P5R cannot recognize such arbitrary I/O device symbols and relay numbers, it is necessary to determine the I/O terminals to which I/O devices are to be connected.
2. The SYSMAC-P5R requires the relay numbers corresponding to the I/O devices for programming. The relay numbers are determined by the locations (I/O terminals) of I/O terminal blocks to which the I/O devices are connected. Each of these relay numbers must be used for ladder diagram programming.
   Output relay coil numbers cannot be used in duplication within the same program.



3.1.3 Determination of internal auxiliary relay numbers

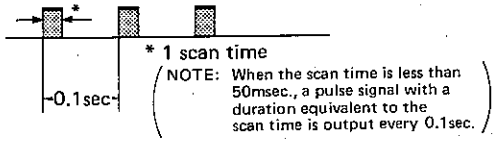
The SYSMAC-P5R incorporates a number of internal auxiliary relays which are used for internal data transfer in sequence circuits. They are independent of I/O devices in sequence. Since the internal auxiliary relays are the data memories incorporated in the CPU, no wiring to the I/O terminals is required. (In other words, they cannot be used as contact outputs.)

- Internal auxiliary relay numbers may not necessarily be assigned consecutively.
- Relay coil numbers cannot be used in duplication within the same program. However, the number of relay contacts is not limited for use.
- If more than the built-in internal auxiliary relays are required, output relays of the output terminals to which output devices are not connected may be used as internal auxiliary relays.

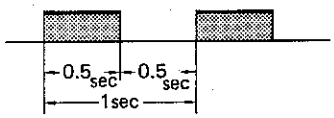
3.1.4 Determination of special auxiliary relay numbers

6 special auxiliary relays are provided. These relays are sort of internal auxiliary relays which operate and release according to the internal conditions controlled by hardware and are independent of the I/O devices in sequence.

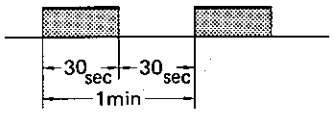
250: This relay is used to generate 0.1sec clock. When used in conjunction with a counter, it functions as a timer for memory retention during a power failure.



251: This relay is used to generate 1sec clock.
When used in conjunction with a counter, it functions as a timer for memory retention during a power failure. The relay output can also be used as a flicker signal.



252: This relay is used to generate 1min clock.
When used in conjunction with a counter, it functions as a timer for memory retention during a power failure.



253: This relay operates when a battery failure occurs and releases when the battery is returned to normal. When this relay operates, the BATTERY FAILURE indicator on the front panel of the CPU illuminates. If the BAT FAULT signal is desired to be transmitted externally, prepare and program a circuit using the contacts of this relay.
(Refer to paragraph 3.3.2, Applied Programs.)

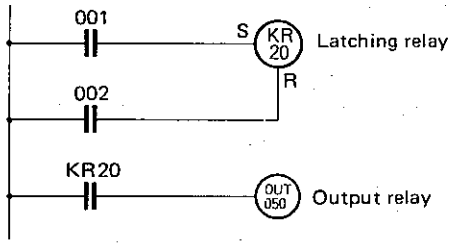
254: This relay operates when a clock failure occurs and releases when the 24-hour clock is returned to normal. To release this relay, push the CLEAR key. If the CLOCK FAULT signal is desired to be transmitted externally, prepare and program a circuit using the contacts of this relay.
(Refer to paragraph 3.3.2, Applied Programs.)

255: This relay is normally in the ON state.

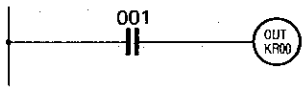
3.1.5 Determination of latching relay numbers

The SYSMAC-P5R has 64 latching relays whose operating states before a power failure can be retained in the memory. Since the operating states of these relays are stored in the memory, all their outputs at the time of the power failure are turned off, but the relays will return to the state before the power failure when power is applied again.

- Relay numbers 00 ~ 63 may not necessarily be assigned consecutively.
- When using a latching relay, the letters "KR" must be prefixed to the relay number. (ex. KR20)
- Relay coil numbers cannot be used in duplication. However, the number of relay contacts is not limited.
- When set and reset input signals are applied simultaneously, the reset input signal takes precedence over the set input signal.
- These relay outputs cannot be transmitted directly to an output terminal. If any of the relay outputs is desired to be transmitted externally, prepare and program a circuit so that the relay output is transmitted externally through an output relay.



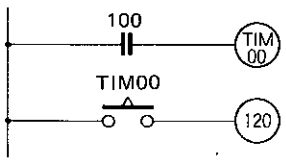
- Latching relays can also be used as auxiliary relays when used with an OUT instruction. However, when the power is turned on to run the CPU, the latching relay does not turn off even if this instruction is executed but operates in the state before the CPU run. Therefore, be sure to perform the all clear operation before using this instruction.



3.1.6 Determination of timer/counter numbers

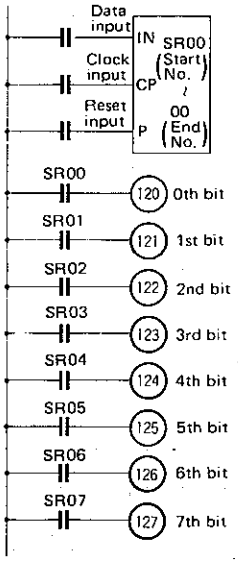
The SYSMAC-P5R has 64 timers and counters which are used for timer/counter numbers in programming.

- Timer/counter numbers 00 ~ 63 are shared by both timers and counters. Therefore, a number already assigned to a timer cannot be used for any other counter.
- The same number will be used for both the coil and contact numbers of a timer or counter. To distinguish timer/counter contact numbers from input relay numbers, shift register and latching relay numbers, the letters "TIM" or "CNT" must be prefixed to each timer/counter contact number (e.g., TIM00, CNT01).



3.1.7 Determination of shift register numbers

The SYSMAC-P5R has 8 shift registers (each consisting of 8 bits). With SR (Shift Register) instructions, the low-order digit always becomes "0" (00, 10, 20, 30, 40, 50, 60, 70). These instructions can be increased or decreased in units of 8 bits. The low-order digit of each bit becomes 0 ~ 7.



- Relay numbers 00 ~ 70 may not necessarily be assigned consecutively.
- Be sure to satisfy the condition; Start No. ≤ End No.
- Shift register coil numbers cannot be used in duplication. However, the number of contacts is not limited.
- When set and reset input signals are applied simultaneously, the reset input signal takes precedence over the set input signal.
- The shift register outputs cannot be transmitted directly to an output terminal. If any of the outputs is desired to be transmitted externally, prepare and program a circuit so that the output is transmitted externally through an output relay.
- Shift registers can also be used as auxiliary relays when used with an OUT instruction. However, when the power is turned on to run the CPU, the shift register does not turn off even if this instruction is executed but operates in the state before the CPU run. Therefore, be sure to perform the all clear operation before using this instruction.

- When using a shift register, the letters "SR" must be prefixed to the relay number (e.g., SR01).

3.1.8 Determination of temporary memory relay numbers

The SYSMAC-P5R has 8 temporary memory relays which are used when plural outputs exist in a block.

- Relay numbers 0 ~ 7 may not necessarily be assigned consecutively.
- Temporary memory relay coil numbers cannot be used in duplication within the same block. With two or more blocks, they can be used in duplication.
- When using a temporary memory relay, the letters "TR" must be prefixed to the relay number (e.g., TR0).

3.2 Instruction Words

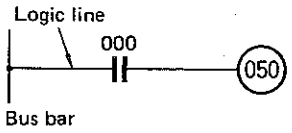
3.2.1 List of instructions

No.	Instruction	Symbol	Function	Word length	Data
1	LOAD	LD	Logical start operation.	1W	• SCY-P5R10E Input relays 000 ~ 047 Output relays 050 ~ 097 Internal auxiliary relays 098 ~ 249 Special auxiliary relays 250 ~ 255 Timers/counters 00 ~ 63 Latching relays 00 ~ 63 Shift registers 00 ~ 77 Temporary memory relays 0 ~ 7 • SCY-P5R30E Input relays 000 ~ 031 Output relays 050 ~ 073 Internal auxiliary relays 074 ~ 249 Special auxiliary relays 250 ~ 255 Timers/counters 00 ~ 63 Latching relays 00 ~ 63 Shift registers 00 ~ 77 Temporary memory relays 0 ~ 7
2	LOAD NOT	LD NOT	Logical NOT start operation.	1W	
3	AND	AND	Logical AND operation.	1W	
4	AND NOT	AND NOT	Logical AND NOT operation.	1W	
5	OR	OR	Logical OR operation.	1W	
6	OR NOT	OR NOT	Logical OR NOT operation.	1W	
7	AND LOAD	AND LD	Logical AND operation with the previous condition.	1W	—
8	OR LOAD	OR LD	Logical OR operation with the previous condition.	1W	
9	OUT	OUT	Outputs the result of a logical operation to the specified output relay, internal auxiliary relay, latching relay or shift register.	1W	• SCY-P5R10E Output relays 050 ~ 097 Internal auxiliary relays 098 ~ 249 Latching relays 00 ~ 63 Shift registers 00 ~ 77 Temporary memory relays 0 ~ 7 • SCY-P5R30E Output relays 050 ~ 073 Internal auxiliary relays 074 ~ 249 Latching relays 00 ~ 63 Shift registers 00 ~ 77 Temporary memory relays 0 ~ 7
10	OUT NOT	OUT NOT	Inverts the results of a logical operation and then outputs them to the specified output relay, internal auxiliary relay, latching relay or shift register.	1W	
11	TIMER	TIM	On-delay timer operation.	2W	Timers/counters 00 ~ 63
12	COUNTER	CNT	Down counter operation.	2W	
13	SHIFT REGISTER	SR	Shift register operation.	2W	Shift registers 00 ~ 77
14	LATCHING RELAY		Latching relay operation.	1W	Latching relays 00 ~ 63
15	TIMER COMPARE	TCM	Used to obtain an arbitrary time from the 24-hour clock.	4W	Time of day 00:00 to 23:59 hours
16	STEP NUMBER	STEP NO	Used to call an arbitrary step number of a step advance program.	2W	Step numbers 01 ~ 99
17	INTERLOCK		Causes all the relay coils between this instruction and the ILC instruction to be reset or not reset according to the result immediately before this instruction.	1W	
18	INTERLOCK CLEAR	ILC	Clears the ILC instruction.	1W	—
19	JUMP	JMP	Cause all the contents of a program between this instruction and the JME instruction to be ignored or executed according to the result immediately before this instruction.	1W	
20	JUMP END	JME	Clears the JMP instruction.	1W	
21	END	END	The end of a program.	1W	

3.2.2 Explanation of instruction words

■ LOAD (LD) & OUTPUT (OUT) INSTRUCTIONS

If each logic line starts with an NO contact, use the LD instruction. Use the OUT instruction for a relay coil.



Coding

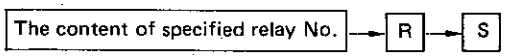
Address	OP	Data
0000	LD	000
0001	OUT	050

Contents of Registers

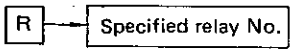
R	S
000	—
000	—

- **Operation of each register**

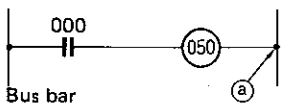
The LD instruction causes the content (ON or OFF state) of the specified relay number to be stored into the RESULT REGISTER (hereafter referred to as "R register"). It also causes the previous result in the R register to be transferred to the STACK REGISTER (hereafter referred to as "S register").



The OUT instruction causes the content of the R register to be output to the specified relay number. In this case, the content of the R register will remain unchanged.



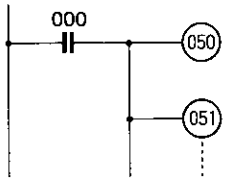
- Bus bar of a different phase is not required to be programmed.



Connection to the bus bar of a different phase (part @) is accomplished automatically by programming an OUT instruction.

- **Consecutive OUT instructions**

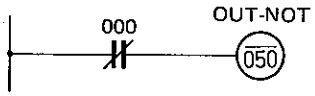
If the OUT instruction is followed by another OUT instruction, this condition is regarded as a circuit error during the program check. However, each output relay operates normally.



OP	Data
LD	000
OUT	050
OUT	051
⋮	⋮

■ LOAD NOT (LD·NOT) & OUTPUT NOT (OUT·NOT) INSTRUCTIONS

If each logic line starts with an NC contact, use the LD·NOT instruction in lieu of the LD instruction. Use the OUT·NOT instruction to invert the output condition.



Coding

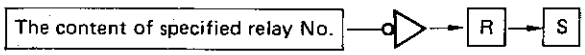
Address	OP	Data
0000	LD·NOT	000
0001	OUT·NOT	050

Contents of Registers

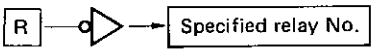
R	S
000	—
000	—

- **Operation of each register**

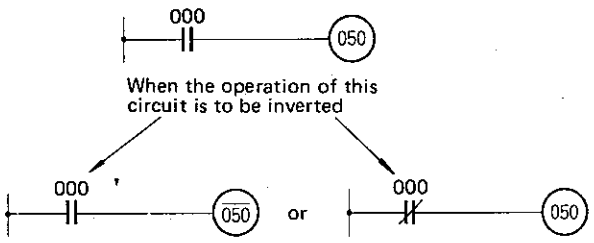
The LD·NOT instruction causes the content of the specified relay number to be inverted and then stored into the R register.



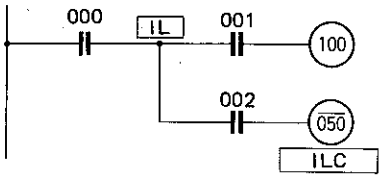
The OUT·NOT instruction causes the content of the R register to be inverted and then output to the specified relay number. In this case, the content of the R register will remain unchanged.



- **Application of OUT·NOT instruction**



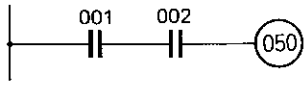
- **Use of OUT·NOT instruction between IL and ILC instructions**



Note that relay 050 operates when the IL condition (000) is OFF.

■ AND INSTRUCTION

NO contacts in series are processed by the AND instruction.



Coding

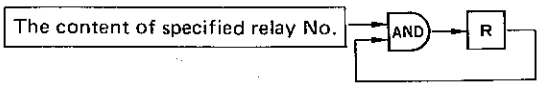
Address	OP	Data
0000	LD	001
0001	AND	002
0002	OUT	050

Contents of Registers

R	S
001	—
001 002	—
001 002	—

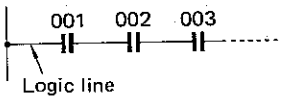
- **Operation of each register**

The AND instruction causes the logical AND operation to be performed between the content of the specified relay number and the content of the R register. The result of the logical AND operation will be newly stored in the R register.



- **Number of contacts**

The number of contacts is not limited for use on a logic line. As many NO contacts as required can be connected by means of the AND key.

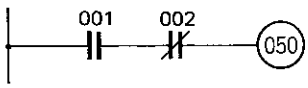


OP	Data
LD	001
AND	002
AND	003
⋮	⋮

In this case, the contact of the first relay number 001 is at the start of each logic line. Therefore, the relay contact must be programmed as "LD001."

■ AND-NOT INSTRUCTION

If an NC contact is connected in series, use the AND-NOT instruction in lieu of the AND instruction.



Coding

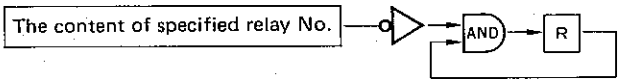
Address	OP	Data
0000	LD	001
0001	AND-NOT	002
0002	OUT	050

Contents of Registers

R	S
001	—
001 002	—
001 002	—

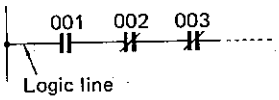
- **Operation of each register**

The AND-NOT instruction causes the content of the specified relay number to be inverted and then ANDed with the content of the R register. The result of the logical AND operation will be newly stored in the R register.



- **Number of contacts**

The number of contacts is not limited for use on a logic line. As many NC contacts as required can be connected in series by means of AND NOT keys.

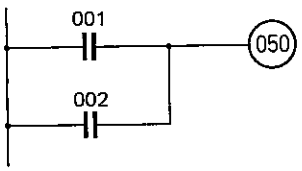


OP	Data
LD	001
AND-NOT	002
AND-NOT	003
⋮	⋮

In this case, the contact of the first relay number 001 is at the start of each logic line. Therefore, the relay contact must be programmed as "LD001."

■ OR INSTRUCTION

NO contacts in parallel are processed by the OR instruction.



Coding

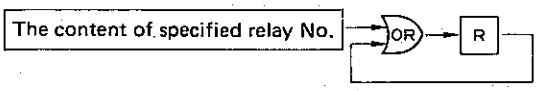
Address	OP	Data
0000	LD	001
0001	OR	002
0002	OUT	050

Contents of Registers

R	S
001	—
001 / 002	—
001 / 002	—

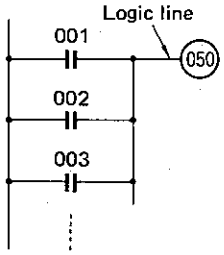
- **Operation of each register**

The OR instruction causes the logical OR operation to be performed between the content of the specified relay number and the content of the R register. The result of the logical OR operation will be newly stored in the R register.



- **Number of contacts**

The number of contacts is not limited for use on a logic line. As many NO contacts as required can be connected by means of the [OR] key.

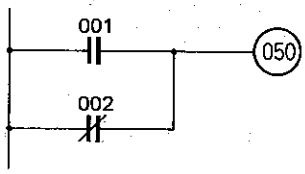


OP	Data
LD	001
OR	002
OR	003
⋮	⋮
OUT	050

In this case, the contact of the first relay number 001 is at the start of each logic line. Therefore, the relay contact must be programmed as "LD001."

■ OR-NOT INSTRUCTION

If an NC contact is to be connected in parallel, use the OR-NOT instruction in lieu of the OR instruction.



Coding

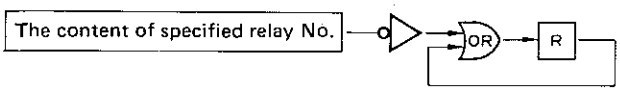
Address	OP	Data
0000	LD	01
0001	OR-NOT	02
0002	OUT	050

Contents of Registers

R	S
001	—
001 / 002	—
001 / 002	—

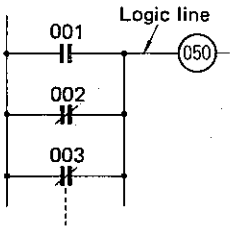
- **Operation of each register**

The OR-NOT instruction causes the content of the specified relay number to be inverted and then ORed with the content of the R register. The result of the logical OR operation will be newly stored in the R register.



- **Number of contacts**

The number of contacts is not limited for use on a logic line. As many NC contacts as required can be connected by means of [OR] [NOT] keys.

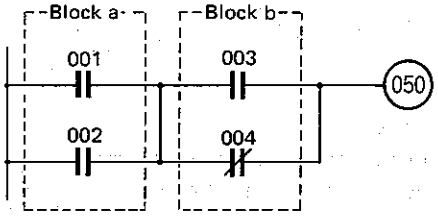


OP	Data
LD	001
OR-NOT	002
OR-NOT	003
⋮	⋮
OUT	050

In this case, the contact of the first relay number 001 is at the start of each logic line. Therefore, the relay contact must be programmed as "LD001."

■ AND-LOAD (AND-LD) INSTRUCTION

For inter-block AND operation between two or more blocks, use the AND-LD instruction.



Coding

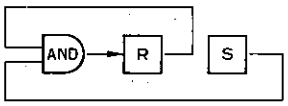
Address	OP	Data
0000	LD	001
0001	OR	002
0002	LD*	003
0003	OR-NOT	004
0004	AND-LD**	
0005	OUT	050

Contents of Registers

R	S
001	—
001 / 002	—
003	001 / 002
003 / 004	001 / 002
001 003 / 002 004	—
001 003 / 002 004	—

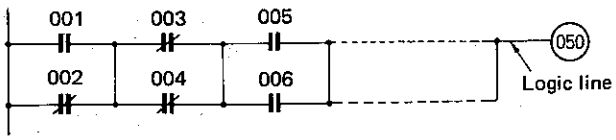
NOTES: * Use this instruction as the first instruction for the next block to be ANDed with the preceding block.
** Use the AND-LD instruction for series connection of two blocks (blocks a and b).

- **Operation of each register**
  1. By the LD001 and OR002 instructions, the result of the logical OR operation in block a is stored into the R register.
  2. By the LD003 instruction in block b, the result of the operation in block a is transferred into the S register, while the result of the logical operation by instructions LD003 and OR·NOT004 in block b is stored into the R register.
  3. AND·LD instruction causes the logical AND operation to be performed between the R register and the S register. The result of the logical AND operation will be newly stored into the R register.



- **Number of blocks**

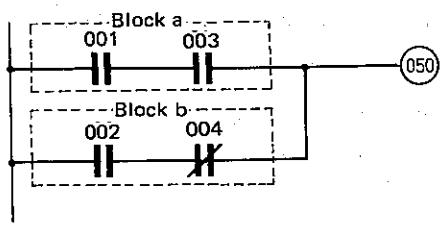
The number of blocks is not limited for AND·LD operation of a logic line. As many blocks as required can be continued for series connection by means of [LD] ~ [AND] [LD] keys.



OP	Data
LD	001
OR·NOT	002
LD·NOT	003
OR·NOT	004
AND·LD	–
LD	005
OR	006
AND·LD	–
⋮	⋮
OUT	050

■ OR·LOAD (OR·LD) INSTRUCTION

For inter-block OR operation between two or more blocks, use the OR·LOAD instruction.



Coding

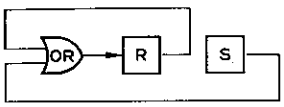
Address	OP	Data
0000	LD	001
0001	AND	003
0002	LD*	002
0003	AND·NOT	004
0004	OR·LD**	
0005	OUT	050

Contents of Registers

R	S
001	—
001 003	—
002	001 003
002 004	001 003
001 003 002 004	—
001 003 002 004	—

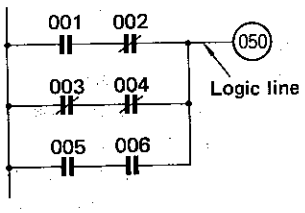
NOTES: * Use this LD instruction as the first instruction of the next block to be ORed with the preceding block.
** Use the OR·NOT instruction for parallel connection of two blocks (blocks a and b).

- **Operation of each register**
  1. By the LD001 and AND003 instructions, the result of the logical AND operation in block a is stored into the R register.
  2. By the LD002 instruction in block b, the result of the operation in block a is transferred into the S register, while the result of the logical operation by instructions LD002 and AND·NOT004 in block b is stored into the R register.
  3. The OR·LD instruction causes the logical OR operation to be performed between the R register and the S register. The result of the logical OR operation will be newly stored into the R register.



- **Number of blocks**

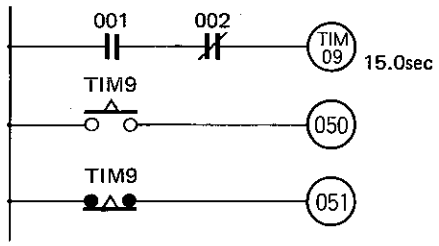
The number of blocks is not limited for OR·LD operation on a logic line. As many blocks as required can be continued for parallel connection by means of [LD] ~ [OR] [LD] keys.

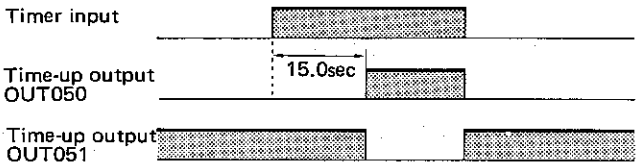


OP	Data
LD	001
AND·NOT	002
LD·NOT	003
AND·NOT	004
OR·LD	–
LD	005
AND	006
OR·LD	–
⋮	⋮
OUT	050

■ TIMER (TIM) INSTRUCTION

The TIM instruction can be used as an ON-delay timer in the same manner as a relay circuit.



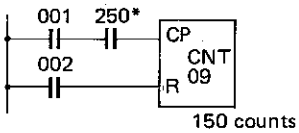


Coding

Address	OP	Data
0000	LD	001
0001	AND-NOT	002
0002	TIM	09*
0003		150**
0004	LD-TIM	09
0005	OUT	050
0006	LD-NOT-TIM	09
0007	OUT	051

NOTES: * Timer number 00 ~ 63.
** Time setting value 000 ~ 999 x 0.1sec.

- **Operation of each register**
  The timer starts when the content of the R register is logical 1 and resets when the content of the R register is logical 0.
- **Number of contacts**
  A time-up contact designates the timer number itself. Both NO and NC contacts can be used in the required quantity.
- **Timer is of decrementing type**
  The timer is of a decrementing type which produces an output when the present value (time remaining) becomes "000." When the timer input is turned off, the present value of the timer returns to the preset value. The timer output is transmitted externally through an output relay as shown in the above circuit example.
- **Timer is reset at the time of a power failure**
  If a power failure occurs, the timer is reset and the present value returns to the preset value. Therefore, if it is required to retain the present value of the timer in the memory, a memory retentive type timer circuit as shown below must be used for programming.
- **Memory retentive type timer**
  A circuit to memorize the present value of the timer during a power failure is configured using a combination of clock instruction and counter (CNT) instruction.

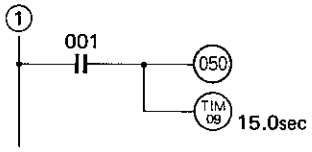


OP	Data
LD	001
AND	250*
LD	002
CNT	09
	150

NOTE: * Special auxiliary relay 250 is for 0.1sec clock.

- **Consecutive OUT instruction and TIM instruction**
  The operations of the circuits ① and ② below are the same, either of which may be used for programming.

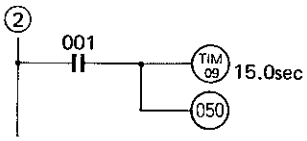
①



OP	Data
LD	001
OUT	050
TIM	09
	150

When the NO contact 001 turns ON, output relay 050 is energized and at the same time timer 09 starts operating.

②

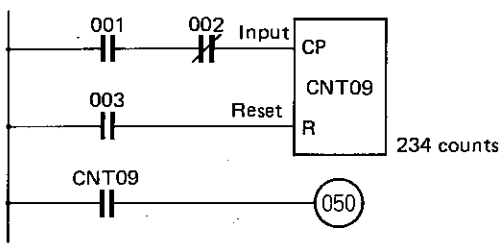


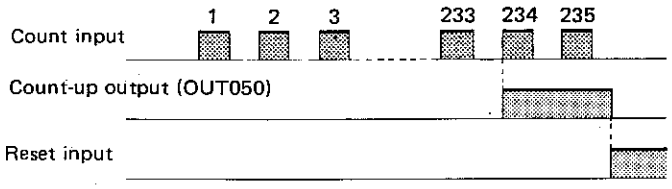
OP	Data
LD	001
TIM	09
	150
OUT	050

When the NO contact 001 turns ON, timer 09 starts operating and at the same time, output relay 050 is energized.

■ COUNTER (CNT) INSTRUCTION

The CNT instruction can be used as a preset counter in the same manner as a relay circuit.



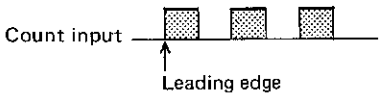


Coding

Address	OP	Data
0000	LD	001
0001	AND-NOT	002
0002	LD	003
0003	CNT	09
0004		234
0005	LD-CNT	09
0006	OUT	050

NOTES: 1. A counter program must be entered in the order of a count input circuit, a reset input circuit and a counter coil.
2. Counter number 00 ~ 63.
3. Counter setting value 000 ~ 999.

- **Operation of each register**
  The counter resets when the content of the R register is logical 1 and is enabled to count when the content of the R register is logical 0. A count input is provided from the S register.
- **Number of contacts**
  A count-up contact designates the counter number itself. Both NO and NC contacts can be used in the required quantity.
- **Counter is of decrementing type**
  The counter is of a decrementing type which produces an output when the count value becomes "000." The present value of the counter returns to the preset value when a reset input is applied. The counter output is transmitted externally through an output relay as shown in the above circuit example.
- After the preset count is up, subsequent count inputs are ignored.
- At the leading edge (i.e., from OFF to ON) of a count input signal, the counter decrements the count value by 1.

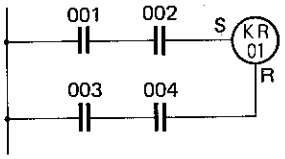


- When both a count input and a reset input are applied simultaneously, the reset input takes precedence over the count input. Even if the reset input is removed after this, the counter performs no counting operation.

- **The present value of the counter is retained in memory during a power failure**
  If a power failure occurs, the counter is not reset and the present value (i.e., count remaining) of the counter is retained in the memory.

■ LATCHING RELAY (KR) INSTRUCTION

The KR instruction can be used as a latching relay in the same manner as a relay circuit.



Coding

Address	OP	Data
0000	LD	001
0001	AND	002
0002	LD	003
0003	AND	004
0004	KR*	01

Contents of Registers

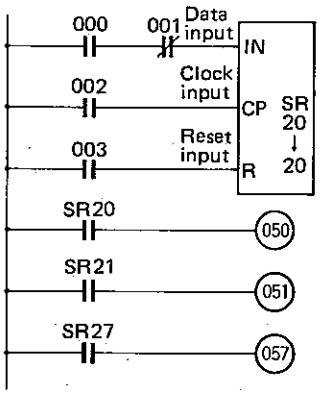
R	S
001	—
001 002	—
003	001 002
003 004	001 002
003 004	001 002

NOTES: * A latching relay program must be entered in the order of a set input circuit, a reset input circuit and a latching relay coil. Use the KR instruction to program a latching relay coil.

- **Operation of each register**
  The latching relay operates when the content of the R register is logical 0 and the content of the S register is logical 1. The relay releases when the content of the R register is logical 1.
- When both a set input and a reset input are applied simultaneously, the reset input takes precedence over the set input.
- The content of the latching relay is retained in the memory during a power failure. It continues to be retained until application of a reset input.

■ SHIFT REGISTER (SR) INSTRUCTION

The SR instruction can be used as a serial input shift register.

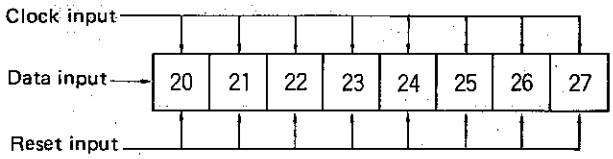


NOTE: A shift register must be programmed in the order of data input, clock input, reset input and SR.

Coding

Address	OP	Data
0200	LD	000
0201	AND-NOT	001
0202	LD	002
0203	LD	003
0204	SR	20
0205		20
0206	LD-SR	20
0207	OUT	050
0208	LD-SR	21
0209	OUT	051
0210	LD-SR	27
0211	OUT	057

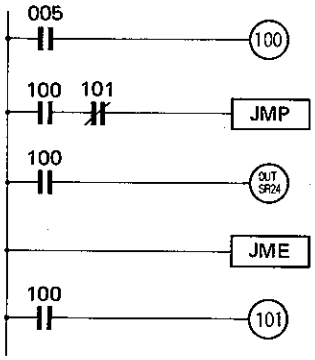
- Each SR instruction must be specified in units of 8 bits. In the above exmaple, 8 bits from SR20 to SR27 are transferred.



- The 8-bit contents of the shift register (SR20 ~ SR27 in the above example) can be output bit by bit using a LD-SR instruction.

- When a reset input is applied to the shift register, 8 bits are reset all together.

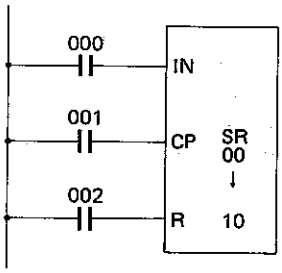
- Any of the 8 bits can be set or reset by force.



OP	Data
LD	005
OUT	100
LD	100
AND-NOT	101
JMP	
LD	100
OUT-SR	24
JME	
LD	100
OUT	101

With a circuit arranged as shown above, a bit in SR24 can be set forcedly when NO contact 005 is turned on. To reset the bit in SR24, use an OUT-NOT-SR instruction.

- Shift register exceeding 8 bits. In this case, a shift register circuit can be configured by combining two or more stages of 8-bit shift registers.



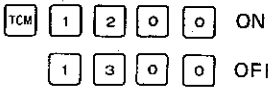
Coding

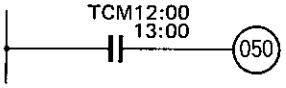
Address	OP	Data
0200	LD	000
0201	LD	001
0202	LD	002
0203	SR	00
0204		10

The above circuit configuration shows a 16-bit shift register from SR00 to SR17. The data 00 for address 0203 indicates SR bits 00 ~ 07 and the data 10 for address 0204 indicates SR bits 10 ~ 17. Accordingly, any shift register configuration is possible by changing each data.

■ TIMER COMPARE (TCM) INSTRUCTION

The TCM instruction can be used when time setting is required for the built-in 24-hour clock. As shown below, output 050 will be ON for a period of time from 12:00:00 to 12:59:59.

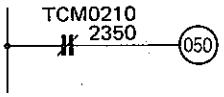




Coding

Address	OP	Data
0200 0201	LD,TCM	1200
0202 0203		1300
0204	OUT	050

- In the above example, if the time of day is 12:30:59 when power is applied, output 050 will be on from the time of the power application until 12:59:59.
- With this instruction, setting of seconds is impossible.
- An ON time set value must be greater than an OFF time set value. If an output is required for a period from 23:50 to 02:10 hours, the time setting must be programmed as shown below using LD·NOT and TCM instructions.



Coding

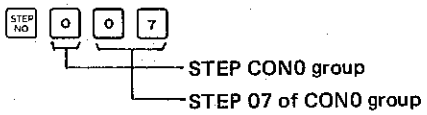
Address	OP	Data
0200 0201	LD·NOT, TCM	0210
0202 0203		2350
0204	OUT	050

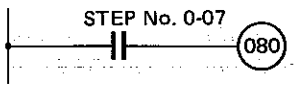
- In the absence of any OFF time set value, the same time as the ON time set value will be set automatically.

NOTE: Refer to paragraph 3.4.16 for the time setting of the 24-hour clock.

■ STEP NUMBER (STEP·NO) INSTRUCTION

The STEP·NO instruction is used to determine as to which step number in a step advance program is presently being executed. In the following example, output 080 will turn on at the step 07 of step controller group 0 (step advance program).





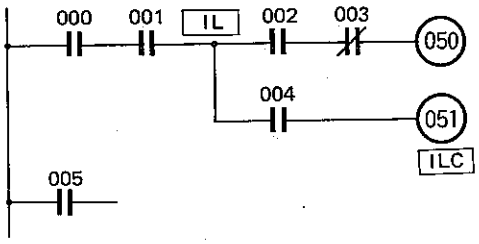
Coding

Address	OP	Data
0200 0201	LD, STEP·NO	007
0202	OUT	080

- Any step of a step controller under execution will be retained in memory when a power failure occurs. Therefore, upon recovery from the power failure, the CPU will restart the operation from the step being executed at the time of the power failure. However, it is possible to program so that the CPU will start from step 01 upon recovery from the power failure. (Refer to paragraph 4.3.7, Applied Programs.)

■ INTERLOCK (IL)/INTERLOCK CLEAR (ILC) INSTRUCTIONS

The IL and ILC instructions are used in pairs when branching a circuit to plural OUT instructions.



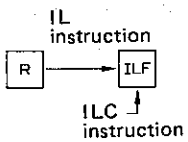
Coding

Address	OP	Data	
0200	LD	000	
0201	AND	001	
0202	IL	—	
0203	LD	002	*
0204	AND·NOT	003	
0205	OUT	050	
0206	LD	004	
0207	OUT	051	
0208	ILC	—	
0209	LD	005	*

NOTE: * When IL and ILC instructions are used in programming, be sure that an LD instruction will always follow the IL and ILC instructions respectively.

- **Operation of register**

The IL instruction causes the content of the R register to be transferred to the interlock flip-flop (ILF). Accordingly, the ILF is set to "0" if the content of the R register is "0" and to "1" if the content of the R register is "1."

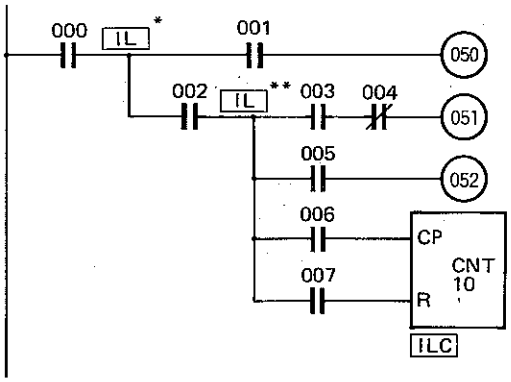


The ILC instruction causes the ILF to be set to "1" irrespective of the content of the R register. In other words, when the IL condition is OFF (i.e., when input 000 or 001 is OFF), the state of each relay between the IL and ILC instructions is as follows.

Output relay, internal auxiliary relay, latching relay or shift register specified by the OUT instruction	OFF
Output relay, internal auxiliary relay, latching relay or shift register specified by the OUT·NOT instruction	OFF
Timer	Resets
Counter, shift register, or latching relay	Holds present state

However, when the IL condition is ON, the state of each relay is the same as that in an ordinary relay circuit without IL/ILC instructions.

- **IL-ILC error**



If IL and ILC instructions are not used in pairs (as in the above example), it is judged as an IL-ILC error during the program check. The operation of the circuit, in this case, will be as programmed, which is shown below.

① If the condition of IL * is OFF, output relays 050, 051 and 052 are all OFF and counter CNT10 retains it present count value.

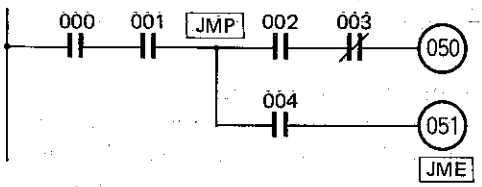
② If the conditions of both IL * and IL ** are OFF, the state of each relay is the same as ①.

③ If the condition of IL * is ON and that of IL ** is OFF, output relay 050 turns ON or OFF if input 001 is ON or OFF and relays 051 and 052 are OFF. Counter CNT10 retains its present count value.

④ If the condition of IL * is OFF and that of IL ** is ON, the state of each relay is the same as ① and ②.

■ JUMP (JMP)/JUMP END (JME) INSTRUCTIONS

The JMP instruction is used in conjunction with the JME instruction and causes the contents of a program between this instruction and the JME instruction to be ignored or executed according to the result immediately before this instruction.



Coding

Address	OP	Data
0200	LD	000
0201	AND	001
0202	JMP	–
0203	LD	002
0204	AND-NOT	003
0205	OUT	050
0206	LD	004
0207	OUT	051
0206	JME	–

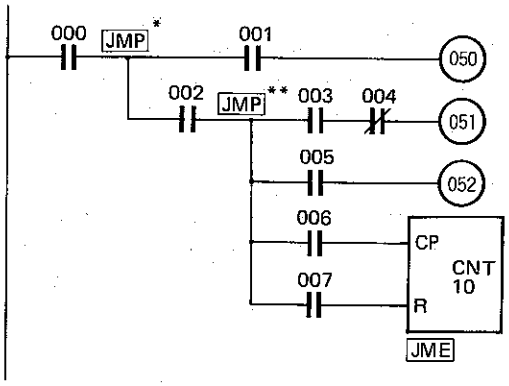
- **Operation of register**

If the content of the R register is "0," the program steps between the JMP and JME instructions are not executed. If the content of the R register is "1," the program steps between the two instructions are executed.
In other words, when the JMP condition is OFF (i.e., when input 000 or 001 is OFF), the state of each relay between the JMP and JME instructions are as follows.

Output relay, internal auxiliary relay	Holds present state
Timer	ditto
Counter, shift register	ditto

However, if the JMP condition is ON, the state of each relay is the same as that in an ordinary relay circuit without JMP/JME instructions.

- **JMP-JME error**



If JMP and JME instructions are not used in pairs (as in the above example), it is judged as an JMP-JME error during the program check. The operation of the circuit, in this case, will be as programmed, which is shown below.

① If the condition of JMP * is OFF, output relays 050, 051 and 052 remain in their present ON/OFF state, and counter CNT10 retains its present count value.

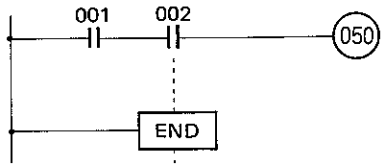
② If the conditions of both JMP * and JMP ** are OFF, the state of each output relay is the same as ①.

③ If the condition of JMP * is ON and that of JMP ** is OFF, output relay 050 turns ON or OFF if input 001 is ON or OFF, and output relays 051 and 052 remain in their present ON/OFF state. Counter CNT10 retains its present count value.

④ If the condition of JMP * is OFF and that of JMP ** is ON, the state of each output relay is the same as ① and ②.

■ END INSTRUCTION

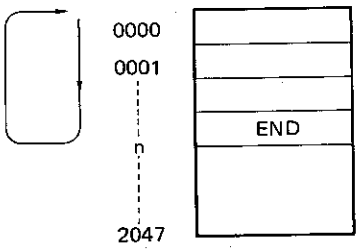
Insert this instruction at the end of a program.



Coding

Address	OP	Data
0000	LD	001
0001	AND	002
0002	OUT	050
0003	⋮	⋮
0004	⋮	⋮
⋮	⋮	⋮
n	END	—

- The program memory of the SYSMAC-P5R is provided with addresses 0000 to 2047. The CPU scans program data from address 0000 to the address with an END instruction according to the sequence diagram.



- When performing a test run, insert an END instruction at each end of a sequence circuit and then delete the END instruction after confirming each circuit. In this manner, the test run can be executed smoothly.

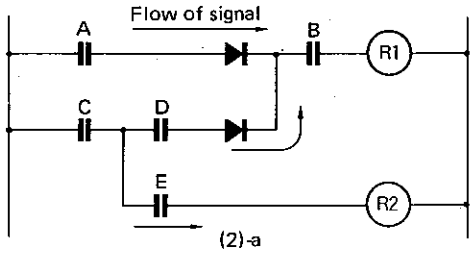
3.3 Programming

3.3.1 How to program

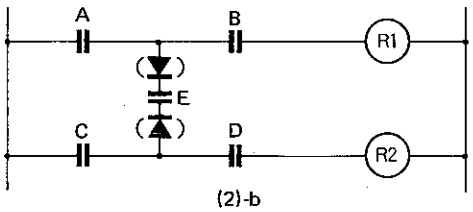
With the SYSMAC-P5R, a sequence circuit is controlled according to the sequence of the instructions stored in the CPU memory. Therefore, it is necessary to observe the hints on correct programming and programming order.

■ HINTS ON CORRECT PROGRAMMING

1. Since the number of contacts is not limited for input/output relays, internal auxiliary relays, timers, etc., it can be said that the best way to design a sequence circuit is to configure a simple, clear circuit, rather than a complicated circuit created by reducing the number of contacts.
2. In the SYSMAC-P5R, signals will flow from the left to the right. In other words, signals will flow as if diodes are inserted in the circuit as shown in (2)-a or (2)-b. To operate a circuit without diodes in the same manner as the circuit configured with general control relays, it is necessary to rewrite the circuit.

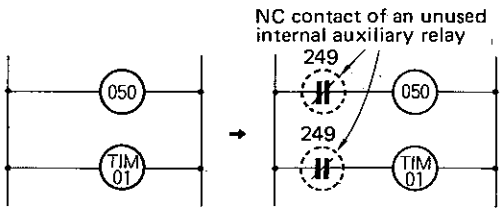


(2)-a

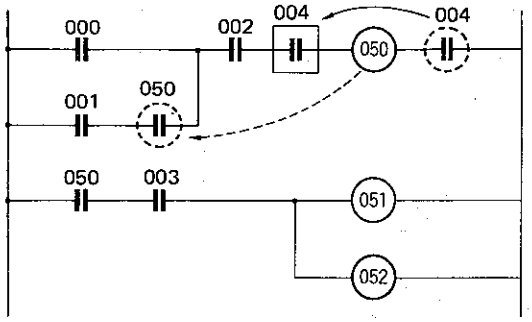


(2)-b

3. In a series-parallel circuit, the number of contacts that can be connected in series is not limited, as well as the number of contacts that can be connected in parallel.
4. No output relay can be connected directly from the bus bar. If necessary, connect it through the NC contact of an unused internal auxiliary relay or special auxiliary relay 255.



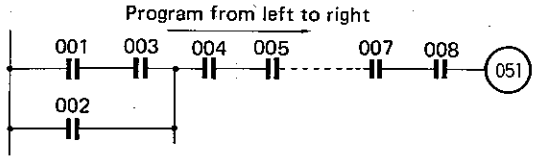
5. All output relays are provided with auxiliary contacts that can be used on a circuit, in addition to the output signal contacts to drive loads actually. The number of contacts that can be used per output relay is not limited.



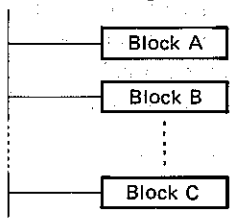
6. No relay contact can be inserted next to an output coil. If necessary, insert it before the output coil.
7. Two or more output coils can be connected in parallel.
8. For contact and coil numbers on the circuit, use the I/O relay numbers described in 3.1.
9. Output coil numbers (including those for timers, counters, shift registers and latching relays) cannot be used in duplication.

■ PROGRAMMING ORDER

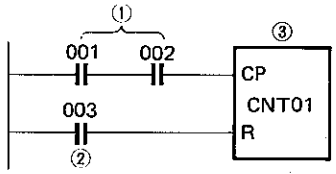
1. Program a circuit from its left to right.



2. Assume the circuit elements located from the bus bar to an output relay as one block. If a number of blocks are in line, programming can be started from any block. However, pay attention in case of circuits utilizing scan time or timing such as differentiator, shift register, etc.



3. When composite instructions such as timer, counter, shift register, latching relay, etc. are used, their order of programming is predetermined. Be sure to perform the programming according to the predetermined order.



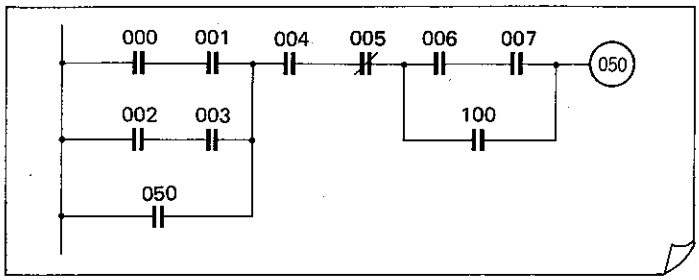
Program in the order of ①→③

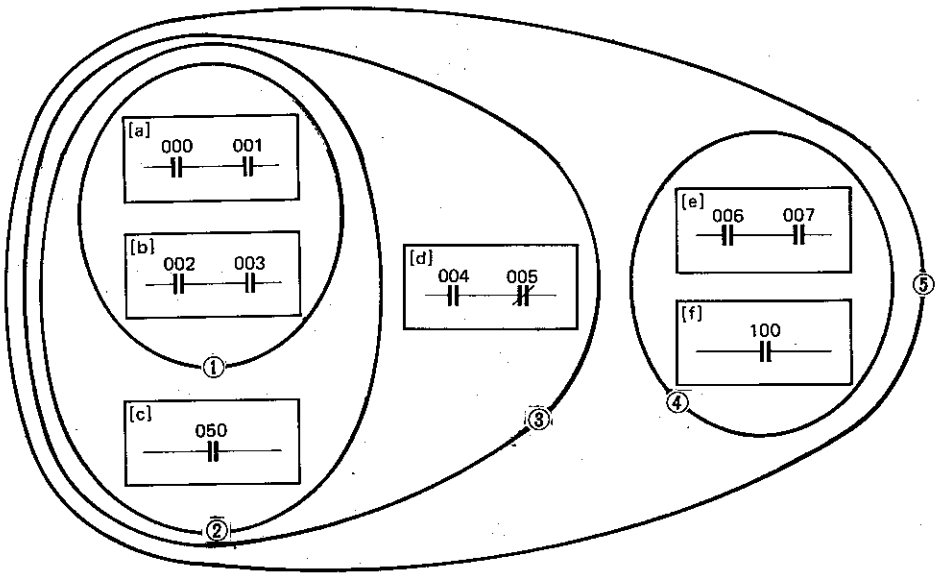
Coding

Address	OP	Data
⋮		⋮
n	LD	001
n + 1	AND	002
n + 2	LD	003
n + 3	CNT	01
n + 4		056
⋮		⋮

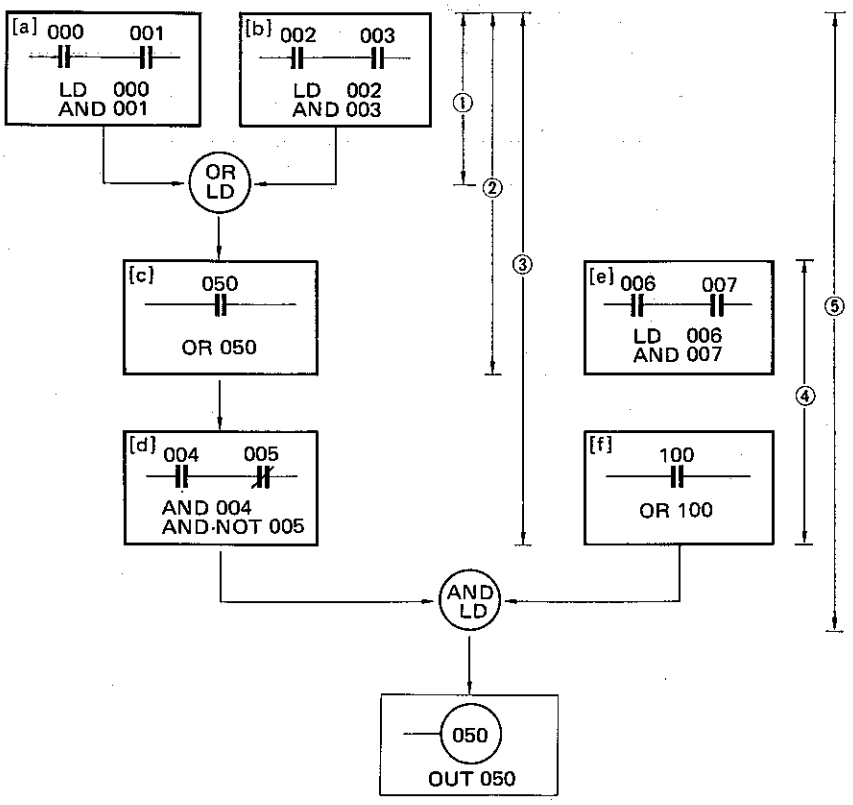
4. Be sure to insert an END instruction at the end of each program.
5. A ladder diagram such as the one shown below can be divided into small blocks as shown below, to program each block in the order of ① to ⑤. Eventually, the circuit will be programmed as one large block such as ⑤.

- **Ladder diagram**





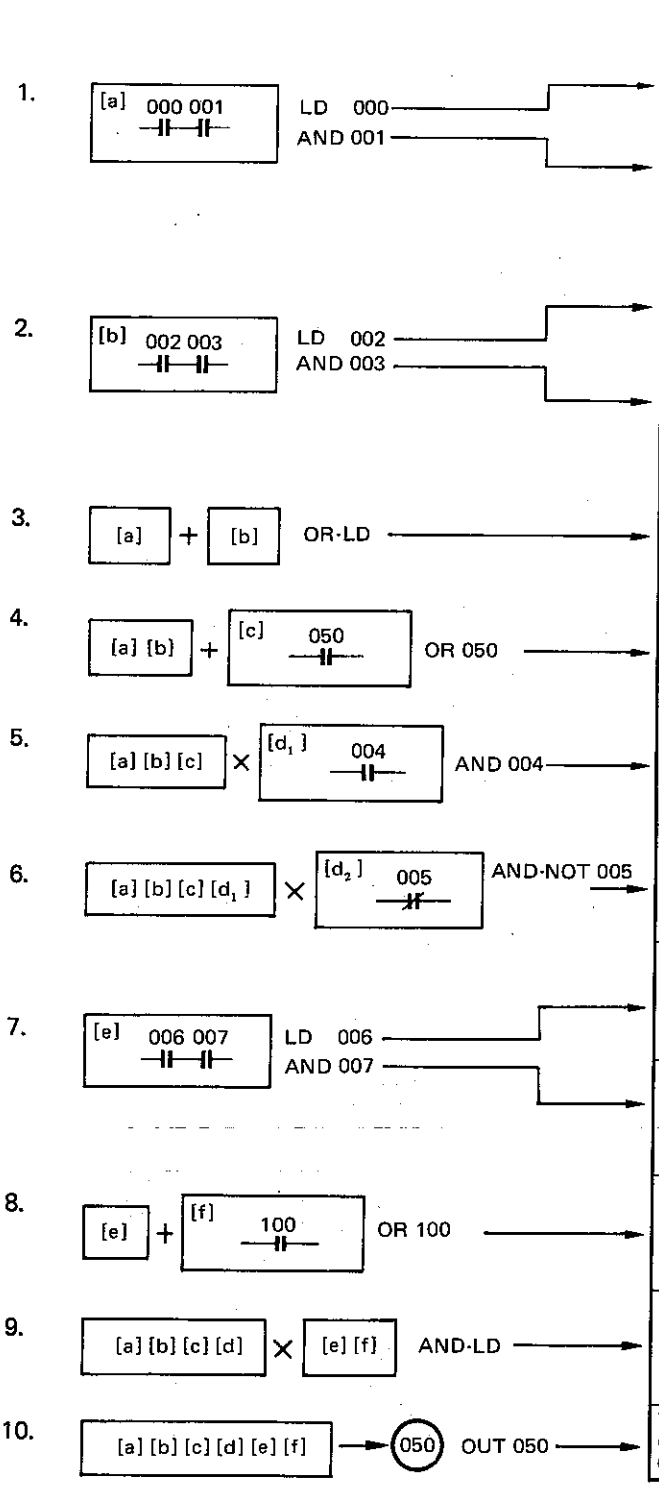
- **Programming procedure**



- **Coding**

Address	OP	Data
0000	LD	000
0001	AND	001
0002	LD	002
0003	AND	003
0004	OR-LD	
0005	OR	050
0006	AND	004
0007	AND-NOT	005
0008	LD	006
0009	AND	007
0010	OR	100
0011	AND-LD	
0012	OUT	050
⋮		⋮
n	END	

- **Operations of R and S registers**

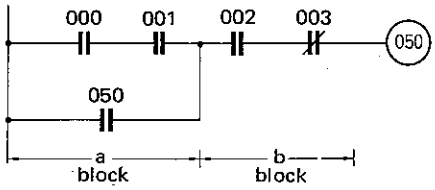


Content of register	R register	S register
The content ("1" or "0") of 000 is stored in R register.	000	Vacant
The content of R register is ANDed with the content of 001 and the result of operation is stored in R register.	Result of 000 001 = [a]	Vacant
The previous content of R register is transferred to S register and the content of 002 is newly stored in R register.	002	[a]
The content of R register is ANDed with the content of 003, and the result of operation is stored in R register.	Result of 002 003 = [b]	[a]
The content of R register (result [b]) is ORed with the content of S register (result [a]), and the result of operation is stored in R register.	Result of ORing [a] with [b] = [a] [b]	Vacant
The content of 050 is ORed with the content of R register, and the result of operation is stored in R register.	Result of ORing [a] [b] with [c] = [a] [b] [c]	Vacant
The content of 004 is ANDed with the content of R register, and the result of operation is stored in R register.	Result of ANDing [a] [b] [c] with [d_1] = [a] [b] [c] [d_1]	Vacant
The content of 005 is ANDed with the content of R register and the result of operation is stored in R register.	Result of ANDing [a] [b] [c] [d_1] with [d_2] = [a] [b] [c] [d]	Vacant
The previous content of R register is transferred to S register, and the content of 006 is stored in R register.	006	[a] [b] [c] [d]
The content of R register is ANDed with the content of 007, and the result of operation is stored in R register.	Result of 006 007 = [e]	[a] [b] [c] [d]
The content of R register is ORed with the content of 100, and the result of operation is stored in R register.	Result of ORing [e] with [f] = [e] [f]	[a] [b] [c] [d]
The content of R register is ANDed with the content of S register, and the result of operation is stored in R register.	[a] [b] [c] [d] [e] [f]	Vacant
The result of R register is output to output relay OUT050.	[a] [b] [c] [d] [e] [f]	Vacant

3.3.2 Applied programs

■ WHEN LD/OR/AND/NOT INSTRUCTIONS ARE USED

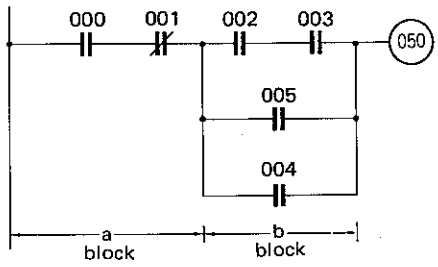
1. An example of parallel-series circuit



OP	Data	
LD	000	a
AND	001	
OR	050	
AND	002	b
AND-NOT	003	
OUT	050	
⋮	⋮	
END		

- Process block b after programming block a (parallel circuit).
- For coding, enter I/O relay numbers in the data field.

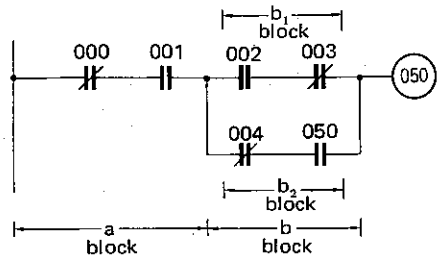
2. An example of series-parallel circuit



OP	Data	
LD	000	a
AND-NOT	001	
LD	002	b
AND	003	
OR	050	
OR	004	
AND-LD		
OUT	050	
⋮	⋮	
END		

- Divide the circuit into blocks a and b and program each block.
- Then combine blocks a and b by AND-LD instruction.

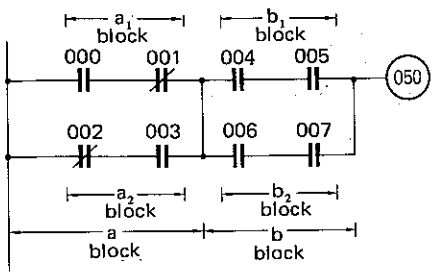
3. An example of series-parallel circuit



OP	Data	
LD-NOT	000	a
AND	001	
LD	002	b_1
AND-NOT	003	
LD-NOT	004	b_2
AND	050	
OR-LD		b_1+b_2
AND-LD		a-b
OUT	050	
⋮	⋮	
END		

- Program block a.
- Program block b_1 and then block b_2.
- Combine blocks b_1 and b_2 using OR-LD instruction.
- Combine blocks a and b using AND-LD instruction.

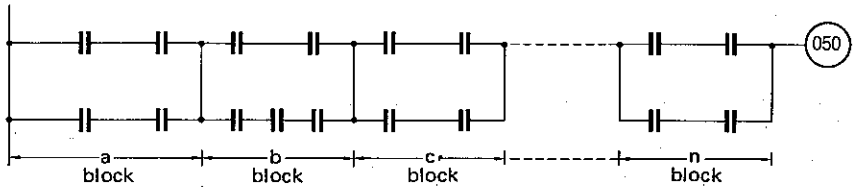
4. An example of connecting parallel circuits in series.



OP	Data	
LD	000	a_1
AND-NOT	001	
LD-NOT	002	a_2
AND	003	
OR-LD		a_1+a_2
LD	004	b_1
AND	005	
LD	006	b_2
AND	007	
OR-LD		b_1+b_2
AND-LD		a-b
OUT	050	
⋮	⋮	
END		

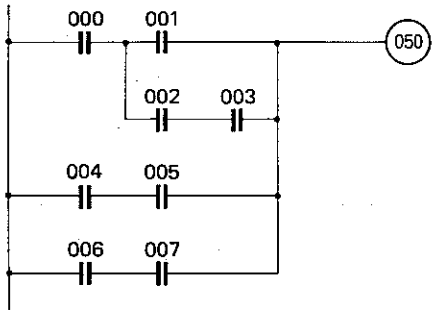
- Program block a_1 and then block a_2 and combine both blocks using OR-LD instruction.
- Program blocks b_1 and b_2 in the same manner as above.
- Combine blocks a and b using AND-LD instruction.

5. An example of connecting parallel circuits in series



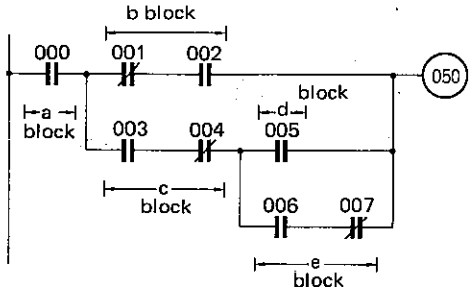
- When a number of blocks continue from block number a to n, the programming procedure is the same as paragraph 4 above. Namely, program the circuit in the following sequence:
  ① block a → ② block b → ③ blocks a·b → ④ block c → ⑤ blocks a·b·c → ⑥ .....

6. An example of complicated parallel circuit



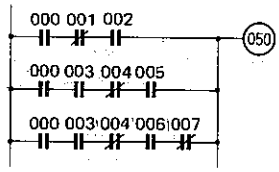
OP	Data
LD	000
LD	001
LD	002
AND	003
OR·LD	
AND·LD	
LD	004
AND	005
OR·LD	
LD	006
AND	007
OR·LD	
OUT	050
⋮	⋮
END	

7. An example of complicated circuit



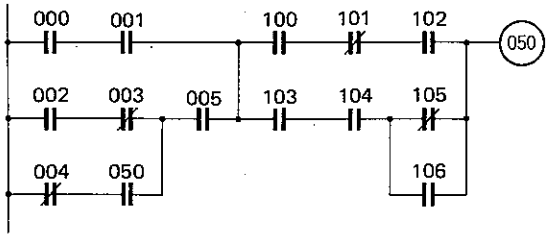
OP	Data	
LD	000	a
LD·NOT	001	b
AND	002	
LD	003	c
AND·NOT	004	
LD	005	d
LD	006	e
AND·NOT	007	
OR·LD		d+e
AND·LD		(d+e)·c
OR·LD		(d+e)·c+b
AND·LD		[(d+e)·c+b]·a
OUT	050	
⋮	⋮	
END		

- The circuit shown on the left may be re-written as follows.



OP	Data
LD	000
AND·NOT	001
AND	002
LD	000
AND	003
AND·NOT	004
AND	005
OR·LD	
LD	000
AND	003
AND·NOT	004
AND	006
AND·NOT	007
OR·LD	
OUT	050
⋮	⋮
END	

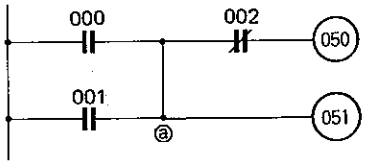
8. An example of complicated circuit



OP	Data
LD	000
AND	001
LD	002
AND·NOT	003
LD·NOT	004
AND	050
OR·LD	
AND	005
OR·LD	
LD	100
AND·NOT	101

OP	Data
AND	102
LD	103
AND	104
LD·NOT	105
OR	106
AND·LD	
OR·LD	
AND·LD	
OUT	050
⋮	⋮
END	

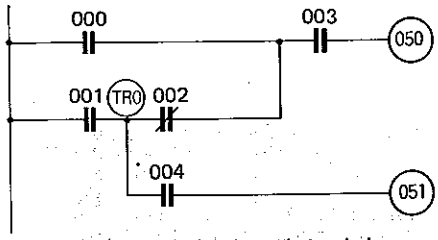
9. An example of circuit requiring caution



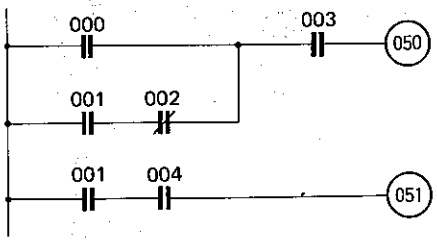
OP	Data
LD	000
OR	001
OUT	051
AND·NOT	002
OUT	050
⋮	⋮
END	

- In such a case as shown above, program relay contact —002— after programming output relay 051. This action is necessary for the following reason. Even if an output is sent to output relay 050, the content of the R register at point@will remain unchanged. However, if —002— is programmed before output relay 050, the content of the R register at point@will change and differ from the content sent to output relay 051.

10. An example of circuit requiring caution



Separate the circuit as shown below.

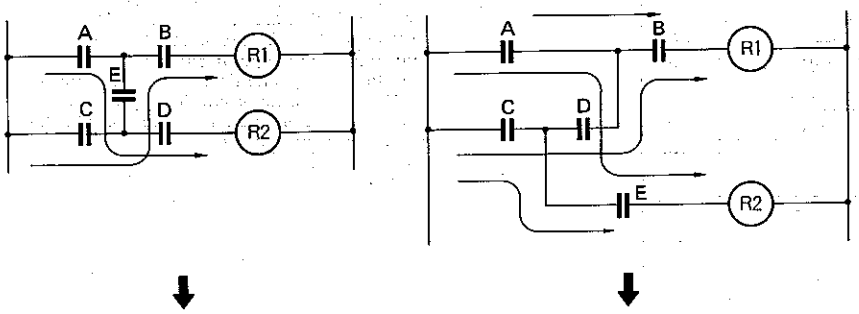


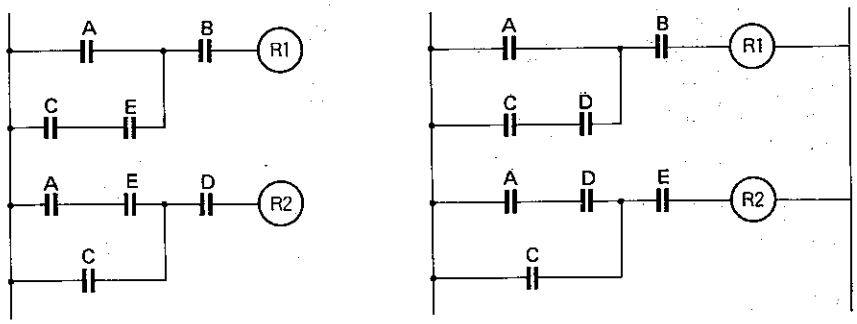
OP	Data
LD	000
LD	001
AND·NOT	002
OR·LD	
AND	003
OUT	050
LD	001
AND	004
OUT	051
⋮	⋮
END	

- If the circuit is to be programmed without separating it, program a temporary memory relay after relay contact —001—. The following table shows an example of programming TR0 after —001—.

OP	Data
LD	000
LD	001
OUT·TR	0
AND·NOT	002
OR·LD	
AND	003
OUT	050
LD·TR	0
AND	004
OUT	051
⋮	⋮
END	

11. Examples of circuit requiring rewrite



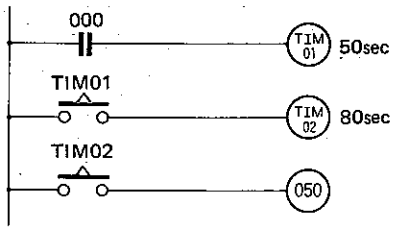


- Such circuits as shown on the upper left cannot be programmed and must therefore be rewritten as shown directly below.
- Since the two upper circuits are respectively configured with control relays, the circuits operate even by the flows of signals shown by the arrows. To permit the similar circuit operation with the SYSMAC-P5R, the two upper circuits must be rewritten into the corresponding circuits shown below.

■ WHEN TIM/CNT INSTRUCTIONS ARE USED

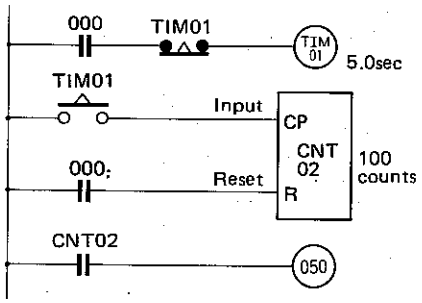
1. Long-time timer

a. Series connection of TIM instructions



OP	Data
LD	000
TIM	01
	500
LD·TIM	01
TIM	02
	800
LD·TIM	02
OUT	050
⋮	⋮
END	

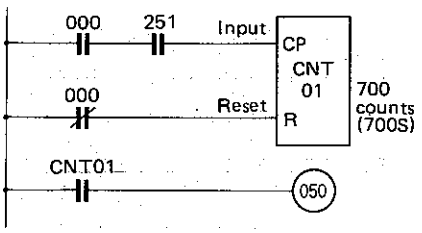
b. Use of CNT instruction (e.g., 500sec)



OP	Data
LD	000
AND·NOT·TIM	01
TIM	01
	050
LD·TIM	01
LD·NOT	000
CNT	02
	100
LD·CNT	02
OUT	050
⋮	⋮
END	

- In this circuit, a pulse is generated every 5 seconds by timer TIM01 and then pulses at intervals of 5 seconds are counted by counter CNT02. The example shown here is a 500sec timer. The setting time of the timer is (timer + scan time) x number of counts.
- The present count value of the counter is retained in memory even if the power switch of the SYSMAC-P5R is turned off.

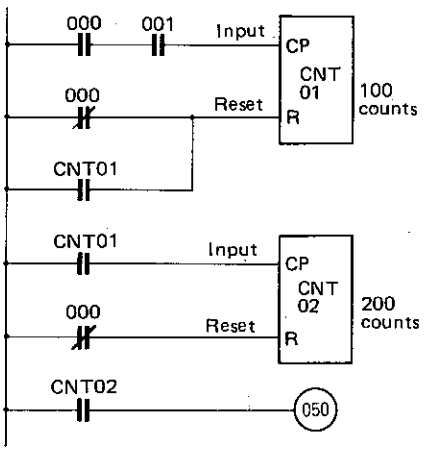
c. Use of internal clock pulse (e.g., 700sec)



OP	Data
LD	000
AND	251
LD·NOT	000
CNT	01
	700
LD·CNT	01
OUT	050
⋮	⋮
END	

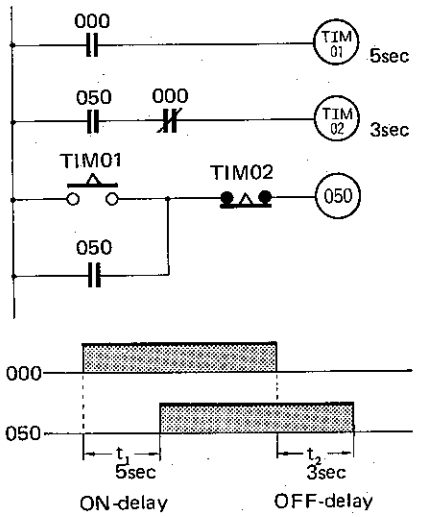
- The SYSMAC-P5R has three types of internal clock pulses (1 min pulse: 252, 1sec pulse: 251, 0.1sec pulse: 250). By counting any of type of pulses with a counter, a long-time timer can be developed.
- As CNT instruction is employed, the present count value is retained in memory even after the power is turned off.

2. Multi-digit counter (e.g., 20,000 counts)



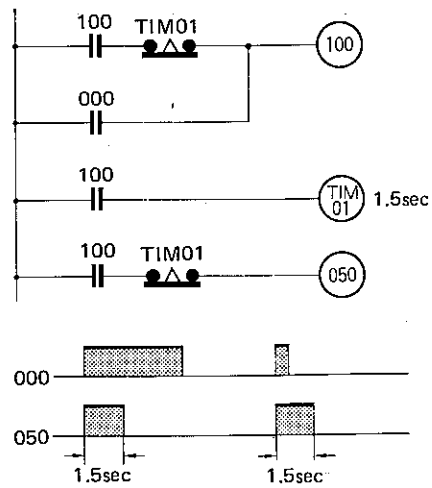
OP	Data
LD	000
AND	001
LD·NOT	000
OR·CNT	01
CNT	01
	100
LD·CNT	01
LD·NOT	000
CNT	02
	200
LD·CNT	02
OUT	050
⋮	⋮
END	

3. An example of ON/OFF-delay timer circuit



OP	Data
LD	000
TIM	01
	050
LD	050
AND·NOT	000
TIM	02
	030
LD·TIM	01
OR	050
AND·NOT·TIM	02
OUT	050
⋮	⋮
END	

4. An example of one-shot timer circuit

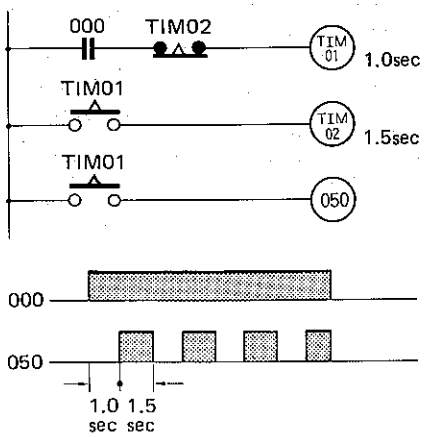


OP	Data
LD	100
AND·NOT	01
OR	000
OUT	100
LD	100
TIM	01
	015
LD	100
AND·NOT·TIM	01
OUT	050
⋮	⋮
END	

- One shot output is produced for only the set time of TIM01 after an input signal is applied. (Input 000 > scan time)

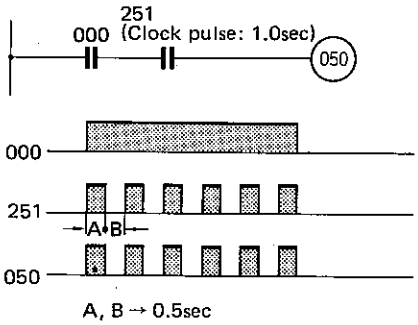
5. Examples of flicker circuit

a. With 2 timers used



OP	Data
LD	000
AND·NOT·TIM	02
TIM	01
	010
LD·TIM	01
TIM	02
	015
LD·TIM	01
OUT	050
⋮	⋮
END	

b. With clock pulse

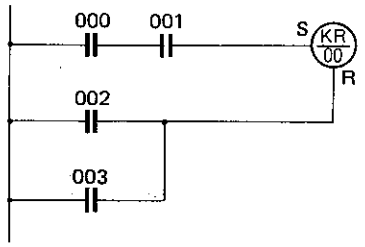


OP	Data
LD	000
AND	251
OUT	050
⋮	⋮
END	

- Using an internal clock pulse (0.1sec, 1.0sec or 1 min), a flicker circuit can be processed easily. In this case, however, the flickering time is available only in the following 3 types.
  Special auxiliary relay number 252:
  1.0 min clock pulse
  Special auxiliary relay number 251:
  1.0sec clock pulse
  Special auxiliary relay number 250:
  0.1sec clock pulse

■ WHEN LATCHING RELAY IS USED

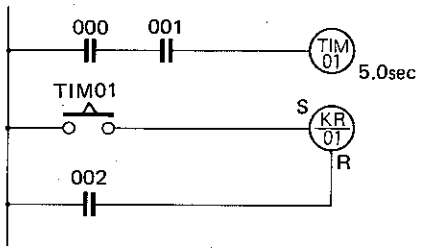
1. Basic circuit



OP	Data
LD	000
AND	001
LD	002
OR	003
KR	01
⋮	⋮
END	

- In the event of a power failure, the ON/OFF state before the power failure can be retained in memory, using a latching relay. SYSMAC-P5R has 64 latching relays with relay numbers KR00 ~ KR63.
- Memory retention time after a power failure is about 1 year just the same as that of the program memory.

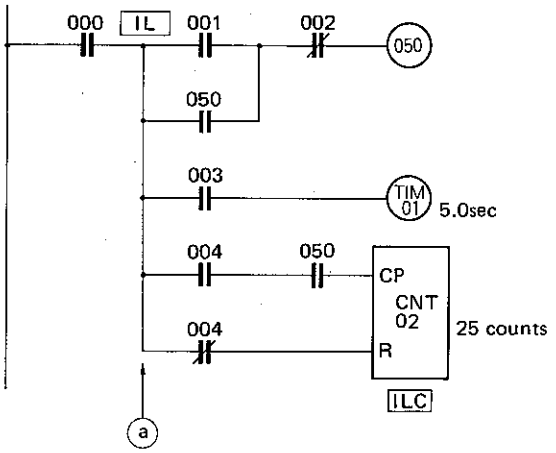
2. A circuit to keep the time-up state



OP	Data
LD	000
AND	001
TIM	01
	050
LD·TIM	01
LD	002
KR	01
⋮	
END	

■ WHEN IL/ILC INSTRUCTIONS ARE USED

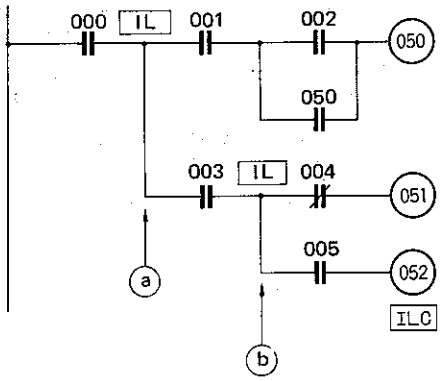
1. Basic circuit



OP	Data
LD	000
IL	
LD	001
OR	050
AND·NOT	002
OUT	050
LD	003
TIM	01
	050
LD	004
AND	050
LD·NOT	004
CNT	02
	025
ILC	
⋮	⋮
END	

- Program the circuit by taking the common line ⓐ after the IL instruction, as a bus bar.
- An ILC instruction must always be added to the end of a circuit employing an IL instruction. The instructions between the IL and ILC instructions are executed.
- When input 000 is OFF, timer TIM01 is reset but the present value of counter CNT02 is retained.
- When preparing an automatic/manual circuit, the circuit shown on the left can be operated only in the automatic mode by turning input 000 on automatically.

2. Output branching circuit

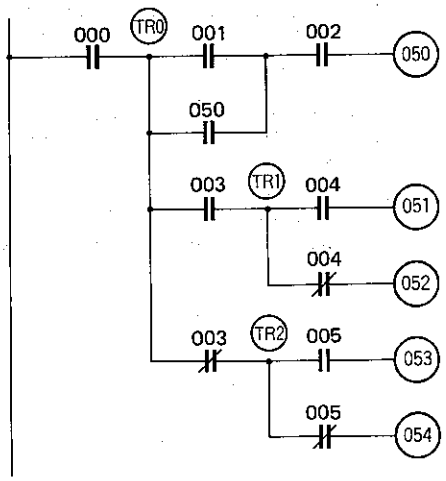


OP	Data
LD	000
IL	
LD	001
LD	002
OR	050
AND-LD	
OUT	050
LD	003
IL	
LD-NOT	004
OUT	051
LD	005
OUT	052
ILC	
⋮	⋮
END	

- IL instructions can be used for programming an output branching circuit (i.e., tree circuit).
- IL instructions can be used in as many stages as required, though this condition is regarded as an IL-ILC error during the program check.
  Each time an IL instruction is programmed, the bus bar changes from ⓐ to ⓑ.

■ WHEN TR INSTRUCTIONS ARE USED

1. Output branching circuit

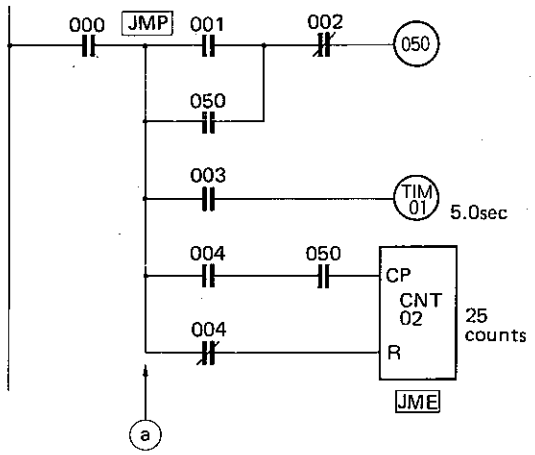


OP	Data
LD	000
OUT-TR	0
LD-TR	0
LD	001
OR	050
AND-LD	
AND	002
OUT	050
LD-TR	0
AND	003
OUT-TR	1
LD-TR	1
AND	004
OUT	051
LD-TR	1
AND-NOT	004
OUT	052
LD-TR	0
AND-NOT	003
OUT-TR	2
LD-TR	2
AND	005
OUT	053
LD-TR	2
AND-NOT	005
OUT	054
⋮	⋮
END	

- In case of an output branching circuit, temporary memory relays (TR0 ~ TR7) are used at each branch point.
- Temporary memory relay coil numbers cannot be used in duplication within the same block. With two or more blocks, they can be used in duplication.

■ WHEN JMP/JME INSTRUCTIONS ARE USED

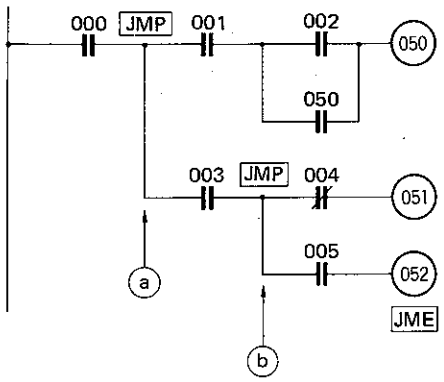
1. Basic circuit



OP	Data
LD	000
JMP	
LD	001
OR	050
AND·NOT	002
OUT	050
LD	003
TIM	01
	050
LD	004
AND	050
LD·NOT	004
CNT	02
	025
JME	
⋮	⋮
END	

- Program the circuit by taking the common line ⓐ after the JMP instruction, as a bus bar.
- A JME instruction must always be added to the end of a circuit employing a JMP instruction.
- When input 000 is ON, the instructions between the JMP and JME instructions are executed.
- When input 000 is OFF, output relay 050, timer TIM01 and counter CNT02 retain their state immediately before the input is turned off.

2. Output branching circuit

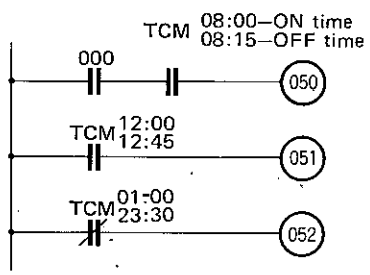


OP	Data
LD	000
JMP	
LD	001
LD	002
OR	050
AND·LD	
OUT	050
LD	003
JMP	
LD·NOT	004
OUT	051
LD	005
OUT	052
JME	
⋮	⋮
END	

- JMP instructions can be used in as many stages as required, although this condition is regarded as a JMP-JME error during the program check.
- Each time a JMP instruction is programmed, the bus bar changes to ⓐ, ⓑ . . . .
- When input 000 is ON, the instructions between the JMP and JME instructions are executed.
- When input 000 is OFF, output relays 050, 051 and 052 retain their ON/OFF state immediately before the input is turned off.

■ WHEN TCM INSTRUCTIONS ARE USED

1. Time signaling circuit

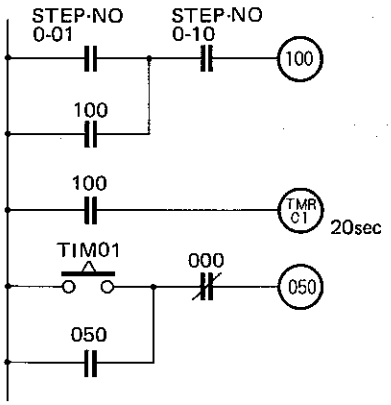


OP	Data
LD	000
AND·TCM	0800
	0815
OUT	050
LD·TCM	1200
	1245
OUT	051
LD·NOT·TCM	0100
	2330
OUT	052
⋮	⋮
END	

- When input signal 000 is ON, output relay 050 operates for a period of time from 08:00 to 08:15 hours.
- With TCM instructions, an ON time must be equal to or less than on OFF time. Therefore, if the time extends over to the following day, a NOT instruction must be used. Output relay 052 operates from 23:00 hours (this day) to 01:00 hours (next day).

■ WHEN STEP-NO INSTRUCTIONS ARE USED

1. Alarm circuit

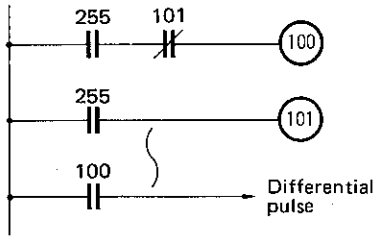


OP	Data
LD-STEP NO	001
OR	100
AND-NOT-STEP NO	010
OUT	100
LD	100
TIM	01
	200
LD-TIM	01
OR	050
AND-NOT	000
OUT	050
⋮	⋮
END	

- A STEP No. instruction is used to call an arbitrary step number in a step advance program.
- In this example of the program for step controller group 0, if the program steps from 01 to 10 are completed within 20 seconds, the program execution is normal. If it takes more than 20 seconds, output relay 050 operates to activate the alarm.

■ 1-CYCLE DIFFERENTIATION

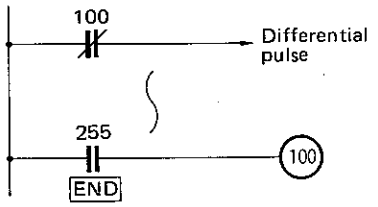
1.



OP	Data
LD	255
AND-NOT	101
OUT	100
LD	255
OUT	101
≀	
LD	100
⋮	⋮
END	

- Special auxiliary relay 255 is normally ON. Shown here is a 1-cycle differentiation circuit when power is applied, using special auxiliary relay 255.

2.

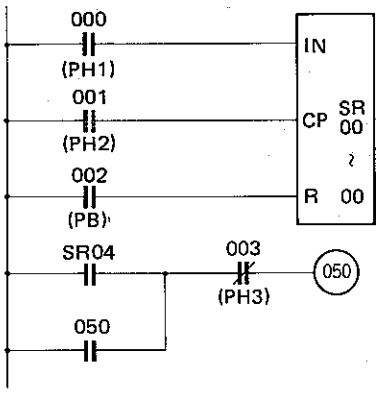


OP	Data
≀	
LD-NOT	100
≀	
LD	255
OUT	100
END	

- Shown here is a 1-cycle differentiation circuit when power is applied, using special auxiliary relay 255. In this case, be sure to program the instruction "OUT100" at the end of the program.

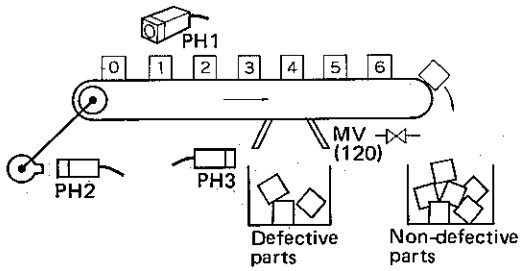
■ WHEN SR INSTRUCTIONS ARE USED

1. Defect detecting circuit (1-stage, 8-bit shift register)

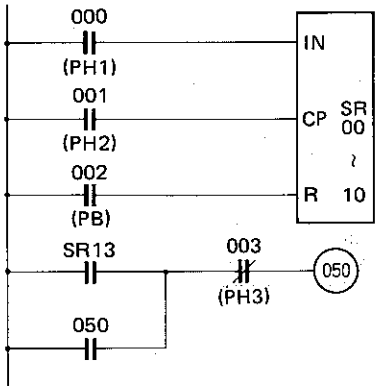


OP	Data
LD	000
LD	001
LD	002
SR	00
	00
LD·SR	04
OR	050
AND·NOT	003
OUT	050
⋮	⋮
END	

- This circuit can be used for such operations in a product inspection line as sorting defective products from non-defective products and distributing them with a cylinder.
- By specifying a shift register as SR00 → 00, shift register bits SR00 to SR07 can be operated to obtain the output of each bit arbitrarily.
- Data in excess of 8 bits are automatically cleared from the first-in data.



2. Multi-stage shift register (2-stage, 16-bit shift register)



OP	Data
LD	000
LD	001
LD	002
SR	00
	10
LD·SR	13
OR	050
AND·NOT	003
OUT	050
⋮	⋮
END	

3.4 Operating Procedure

3.4.1 Basic functions

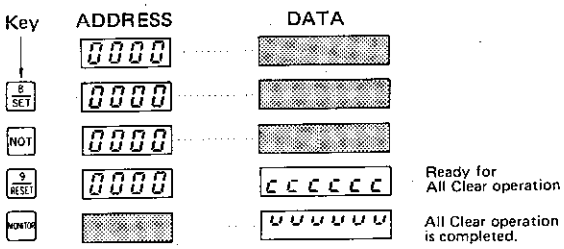
Items of Operation	Description
All program clear	Since the CPU retains previously stored data in memory (by battery back-up), all the memory contents must be cleared to write a new program into the memory.
Address setting	Address setting is required to designate an address in such operations as program read, program write, etc.
Program write	This operation is to store a program in the specified memory address.
Program read	This operation is to confirm whether or not data has been programmed properly in the specified memory address.
Program check	This operation is to confirm whether or not the program data written into the CPU memory through the program console are in agreement with the pre-determined rules (syntax).
RUN	This operation is to place the SYSMAC-P5R in the RUN (Program Execution) state.
Monitor	This operation is to display the operating state of each relay, the operating state of each bit in the shift register, the operating state of a latching relay, or the present value of each timer or counter during the execution of a program.
Trace (continuity) check	When a circuit operation is to be checked in a program simulation or test run, this operation allows the operating state of each relay number to be displayed while tracing the programming sequence of the circuit.
Forced set/reset	This operation is to set or reset by force the operating state of a latching relay, the operating state of each bit in the shift register and the present value of a timer or counter during the execution of a program.
Instruction search	When a circuit change is to be made in a program simulation or test run, this operation allows an address where an instruction or relay number has been written in a program to be searched.
Contact (coil) number change	This operation is to change contact (or coil) number(s) in a program due to a circuit modification.
Contact (coil) addition	This operation is employed when contact (or coil) number(s) is to be added due to a circuit modification.
Contact (coil) deletion	This operation is to change contact (coil) number(s) from a program due to a circuit modification.
Set value change for timer/counter	This operation is to change the set value of a timer or counter during the execution of a ladder diagram program.
24-hour clock time setting	This operation is to correct or advance the time indicated by the 24-hour clock.

3.4.2 All program clear operation

Since the CPU retains previously stored data in memory (by battery back-up), all the memory contents must be cleared to write a new program into the memory.

- **Operating procedure**

- **Display**



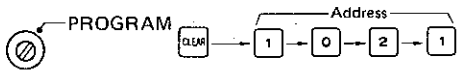
NOTES:
1. By the All Clear operation, all the programs (I/O relays, internal auxiliary relays, latching relays, timers and counters) stored in the memory are cleared.
2. Before the key operation, change the mode selector switch position from "PROM WRITER" to "PROGRAM."
3. In the All Clear operation, a beep sound is generated at the depression of each key.
4. Upon depression of the MONITOR key, the ADDRESS display is extinguished. Subsequent depression of the CLEAR key will cause the ADDRESS display to indicate "0000."

CAUTION:
After the PROGRAM mode selection, depression of the CLEAR key or any key other than the four keys shown above will not allow All Clear operation to be executed. In this case, repeat the operation starting from the mode selection.

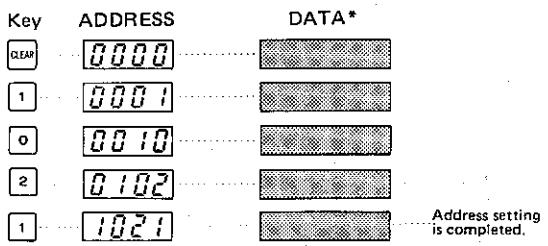
3.4.3 Address setting operation

Address setting is required to designate an address in such operations as program read, program write, etc.

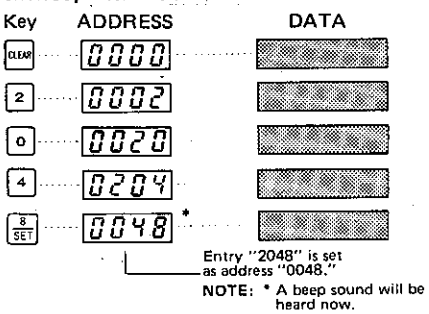
- **Operating procedure**



- **Display**



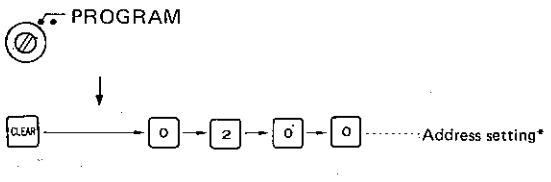
NOTES:
1. Each address is set in 4 digits using numeric data. To set address "0000," no numeric entry is required. To set address "0003," depress only numeric key 3 and to set address "0023," depress only numeric keys 2 and 3. Preceding zero(s) may be omitted from key entry.
2. * The data entered will not be displayed by the address setting operation alone. To display the data entered, ↑ ↓ keys must be depressed.
3. In address setting, when numeric data entered as an address exceeds the max. memory capacity, the first two digits of the 4-digit address are automatically processed as "0." Since the CPU does not recognize this as an error, the only way to identify this error is through confirmation by the operator. For example, with the SCY-P5R10E, if address 2048 is entered, it will be set as follows.



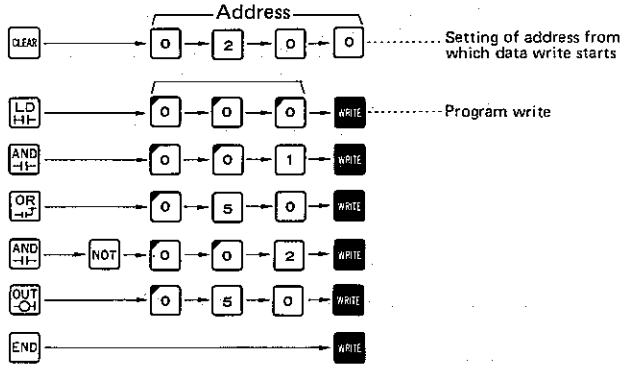
3.4.4 Program write operation

This operation is to store a program in the specified memory address.

- **Operating procedure**

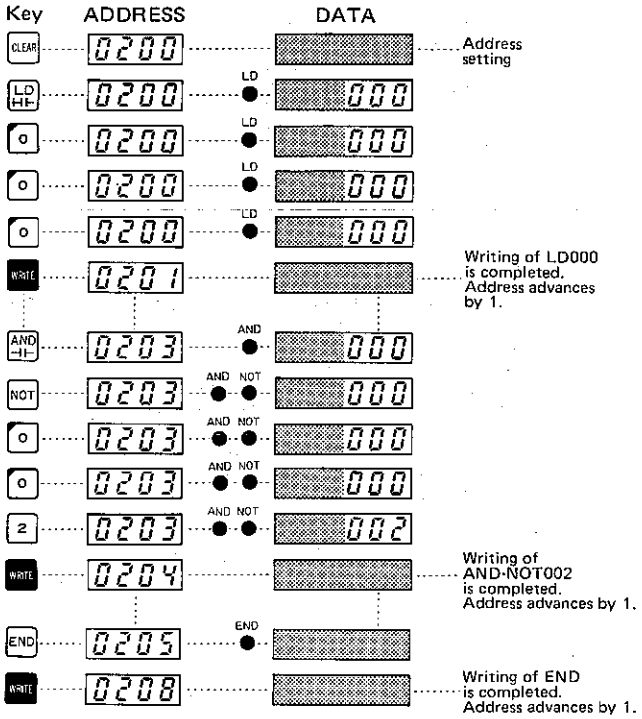


NOTE: * When writing a program from address "0000," no address setting is required.

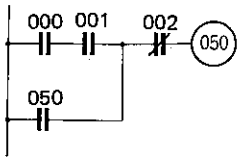


NOTE: The zero key marked [0] may or may not be depressed.

- **Display**



- **Circuit for exercise and programming example**



Address	OP	Data
0200	LD	000
0201	AND	001
0202	OR	050
0203	AND-NOT	002
0204	OUT	050
0205	END	

NOTES:

1. At each depression of the WRITE key, the data appearing on the OP and DATA displays are written into memory.
2. When the WRITE key is depressed in the following cases, a beep sound is generated to signal an erroneous key operation.
   ① When the key is depressed in other than the PROGRAM mode.
   ② When a symbolic or numeric entry error exists (numeric entry error is applicable only when an SR instruction is used).
3. When the WRITE key is depressed in the following cases, a beep sound is generated to signal the requirement of a program change.
   ① When an overflow exists (no space for one word exists in the last address where changing a one-word instruction to a 2-word instruction).
   ② When attempt is made to write an instruction with more than 2-word length into the last address.

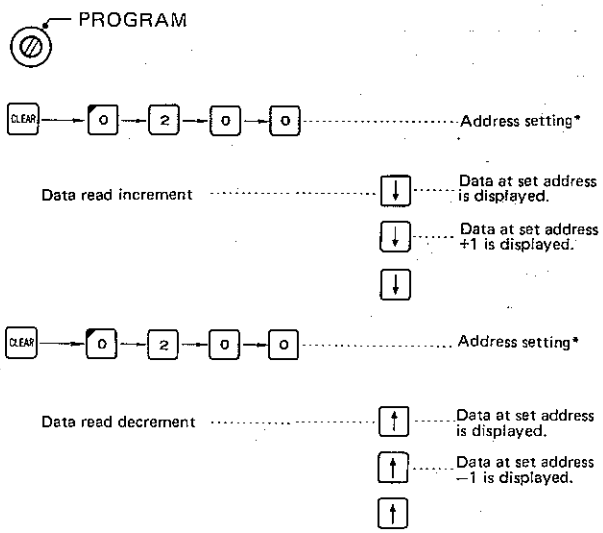
Correction Procedures when an error occurs in program write

1. If an error in programming is noticed before depressing the WRITE key, depress the CLEAR DISPLAY key and the re-entry operation becomes effective.
2. If an error in programming is discovered after depressing the WRITE key, repeat the operation from the address setting, or return to the address in which the error exists by depressing the [↑] key and then depress the CLEAR DISPLAY key and the re-entry operation becomes effective.

3.4.5 Program read operation

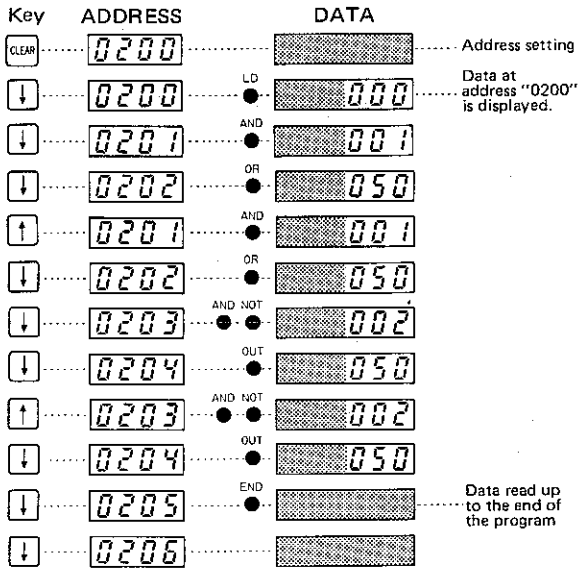
This operation is to confirm whether or not the data has been programmed properly in the specified memory address.

- **Operating procedure**

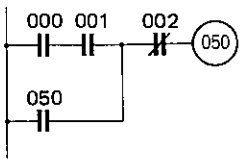


NOTES: 1. When reading a program from address "0000," no address setting is required.
2. The zero key marked [0] may or may not be depressed.

- **Display**



- **Circuit for exercise and programming example**



Address	OP	Data
0200	LD	000
0201	AND	001
0202	OR	050
0203	AND·NOT	002
0204	OUT	050
0205	END	

NOTES:
1. At each depression of the ↓ key, the data at the set address +1 is displayed (i.e., data read increment). However, when the address reaches 2047, a beep sound is generated at each depression of the ↓ key.
2. At each depression the ↑ key, the data at the set address −1 is displayed (i.e., data read decrement). However, when the address reaches 0000, a beep sound is generated at each depression of the ↑ key.

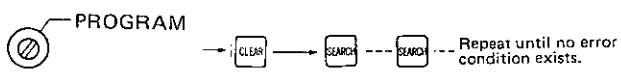
3.4.6 Program check operation

This operation is to confirm whether or not the program data written into the CPU memory through the program console are in agreement with the predetermined rules (syntax) for each programming system.

Items subject to program check are as follows.

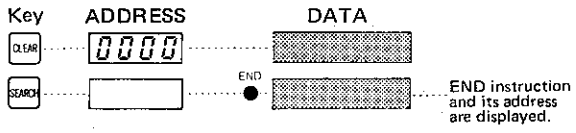
- Coil duplication error
- Circuit error
- IL-ILC error
- JMP-JME error
- Format error
- END instruction missing error

- **Operating procedure**

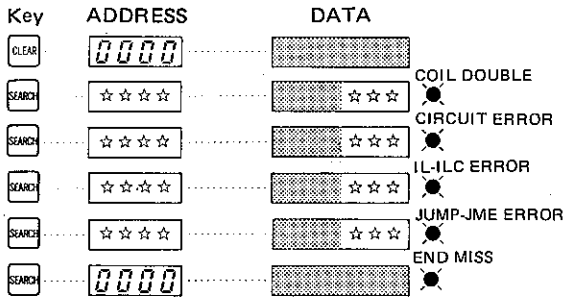


- **Display**

When a program error does not exist



When a program error exists



- **Error conditions**

1. Coil duplication error
   The "COIL DOUBLE" indicator illuminates when the OUT, OUT·NOT, OUT·SR, OUT·NOT·SR, OUT·KR, OUT·NOT·KR, SR, KR, TIM or CNT instructions of the same relay number are contained in a program.
2. Circuit error
   The R register and S register are controlled by computing a difference between the number of logical start instructions (LD and LD·NOT) and the number of interblock logical instructions (AND·LD and OR·LD). If the difference is abnormal according to the nature of the instructions used when the result (OUT, OUT·NOT, OUT·SR, OUT·NOT·SR, OUT·KR, OUT·NOT·KR, CNT, TIM, SR, or KR) is executed, it is regarded as a circuit error, and the "CIRCUIT ERROR" indicator illuminates.
3. IL-ILC error
   IL and ILC instructions must be used in pairs. If this rule is not observed, the "IL-ILC ERROR" indicator illuminates.
4. JMP-JME error
   JMP and JME instructions must be used in pairs. If this rule is not observed, the "JMP-JME ERROR" indicator illuminates.
5. Format error
   If any instruction not conforming with the format (syntax) is found during a program check, the "FORMAT ERROR" indicator illuminates.
6. END instruction missing error
   In the absence of an END instruction at the end of a program, the "END MISS" indicator illuminates.

NOTES:
1. If any programming error is discovered, correct the erroneous program in accordance with the program write procedure.

2. A circuit error is detected by taking that portion of the circuit from the LD-LD-NOT instruction after an OUT instruction to the next OUT instruction as a unit subject to detection.
3. Even if any of the following errors occurs, the CPU can still perform the RUN or MONITOR operation. However, be sure to correct the error to execute the proper program.
   ① Coil duplication error
   ② Circuit error
   ③ IL-ILC error
   ④ JMP-JME error
4. Should any of the following errors occur, the CPU can perform neither the RUN nor MONITOR operation.
   ① Format error
   ② END instruction missing error
   Be sure to correct the erroneous program.

3.4.7 RUN operation

This operation is to place the SYSMAC-P5R in the RUN (Program Execution) condition.

- **Operating procedure**

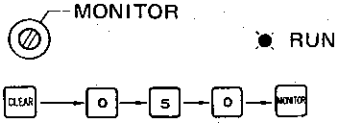
NOTES:
1. In the absence of an END instruction in a program, the RUN indicator will not illuminate even if the operation mode of the CPU is changed to "RUN." (All keys become inoperative.) At the same time, the "END MISS" indicator illuminates and the alarm buzzer sounds. In this case, change the operation mode to "PROGRAM" and enter an END instruction to correct the program.
2. After the CPU starts operating, if an error occurs as a result of a parity check or watchdog timer check, the RUN indicator goes out and the following conditions take place.
   (1) If a parity error occurs, the MEMORY FAILURE indicator illuminates and the memory/CPU fault output (control I/O relay) is ON and the ON/OFF states of all external outputs are held as is.
   (2) If a watchdog timer error occurs, the CPU FAILURE indicator illuminates and the memory/CPU fault output (control I/O relay) is ON and all external outputs are turned off.
   Refer to 7.4, Troubleshooting for details.
3. In other than the RUN and MONITOR modes, all external outputs are turned off. When the mode selector switch position is changed from other mode to "RUN," the SYSMAC-P5R is placed in the same state when power is applied.

3.4.8 Monitor operation

This operation is to display the operating state of each relay, or the present value of each timer or counter during the execution of a program.

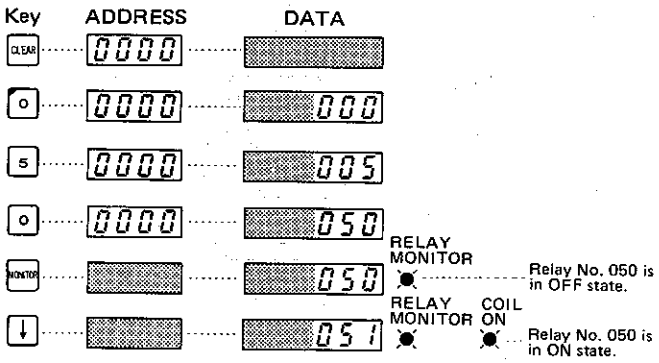
■ MONITORING OF THE OPERATING STATE OF AN INPUT/OUTPUT RELAY OR INTERNAL AUXILIARY RELAY

- **Operating procedure**



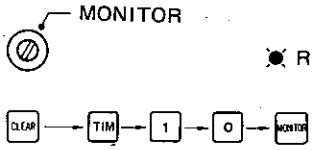
NOTE: The zero key marked [0] may or may not be depressed.

- **Display**

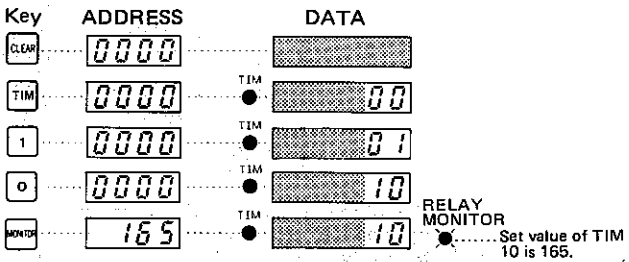


■ MONITORING OF THE CURRENT VALUE OF A TIMER OR COUNTER

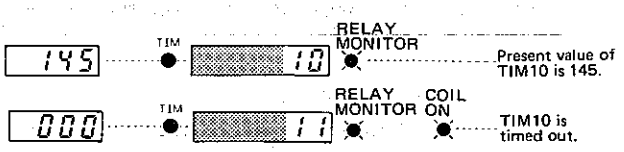
- **Operating procedure**



- **Display**

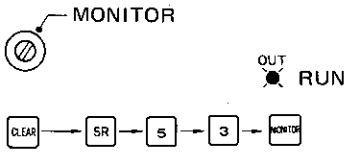


[When the specified timer starts operating, the set time indicated on the ADDRESS display also starts to be decremented toward "0000," while indicating the present value (i.e., remaining time.)]

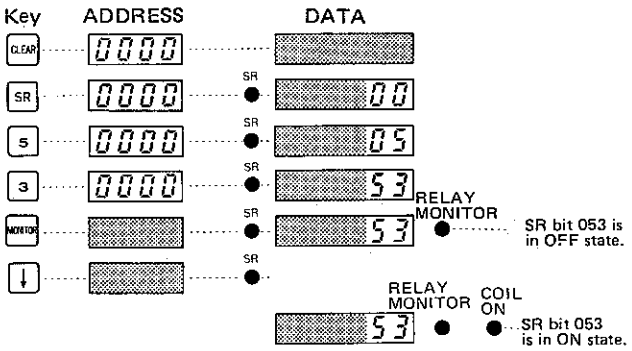


■ MONITORING OF THE OPERATING STAGE OF A SHIFT REGISTER OF LATCHING RELAY

- **Operating procedure**

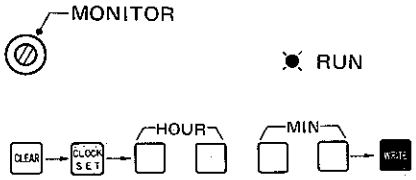


- **Display**



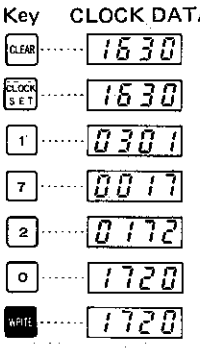
■ TIME CORRECTION OF THE 24-HOUR CLOCK

- **Operating procedure**



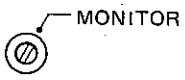
- **Display**

(Example) To change 16:30 to 17:20 hours



■ TIME ADVANCEMENT OF THE 24-HOUR CLOCK

- **Operating procedure**

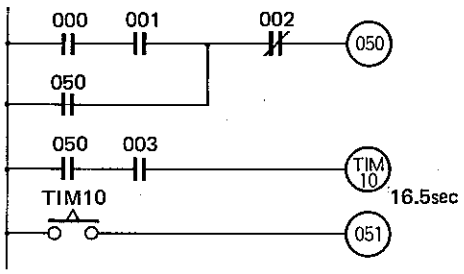


(Example) Time unit of 1 minute converted to 1 second

(Example) Time unit of 1 minute converted to 2 seconds

NOTES:
1. To return the advanced time to normal, depress the CLEAR key.
2. When the time of day is advanced, the "CLOCK FAILURE" indicator illuminates. Depress the CLEAR key to extinguish the indicator.

- **Circuit for exercise and programming example**



Address	OP	Data
0200	LD	000
0201	AND	001
0202	OR	050
0203	AND-NOT	002
0204	OUT	050
0205	LD	050
0206	AND	003
0207	TIM	10
0208		165
0209	LD-TIM	10
0210	OUT	051
0211	END	

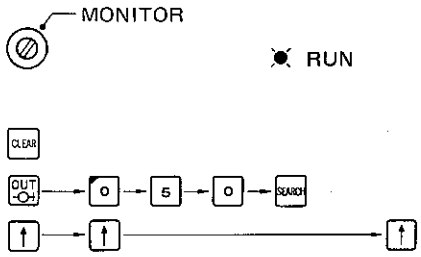
NOTES:
1. The operating state of each I/O relay, internal auxiliary relay, or latching relay is indicated by the "COIL ON" indicator (LED). This indicator illuminates when the state of the specified relay No. is ON and goes out when the state of the specified relay No. is OFF.
2. The present value of each timer or counter is indicated digitally on the ADDRESS display. When the set time of the specified timer has elapsed (or the set count of the specified counter is up), the "COIL ON" indicator illuminates.
3. The operating state of each shift register bit is indicated by the "COIL ON" indicator. This indicator illuminates when the state of the specified bit number is ON and goes out when the state of the specified bit number is OFF.
4. Each depression of the ↓ or ↑ key subsequent to the depression of the MONITOR key causes a relay number, timer/counter number, SR bit number, or KR bit number to be incremented or decremented by 1. Thus, the operating states of relays can be monitored consecutively.
5. When the MONITOR key is depressed in the following cases, a beep sound is generated to alert the operator. Check for the proper operating procedure.
   ① In other than MONITOR mode.
   ② When a symbolic or numeric error exists.
   ③ When an instruction other than OUT, OUT-NOT, OUT-NOT-SR, OUT-SR, OUT-KR, OUT-NOT-KR, TIM, CNT, SR and KR is used.
6. When the relay number reaches the upper limit during the monitor operation, each depression of the ↓ key causes a beep sound to be generated to alert the operator. Check for the proper operating procedure.
7. When the relay number becomes 0 during the monitor operation, each depression of the ↑ key causes a beep sound to be generated to alert the operator. Check for the proper operating procedure.

3.4.9 Trace (continuity) check operation

When a circuit operation is to be checked in a program simulation or test run, this operation allows the operating state of each relay number to be displayed while tracing the programming sequence of the circuit.

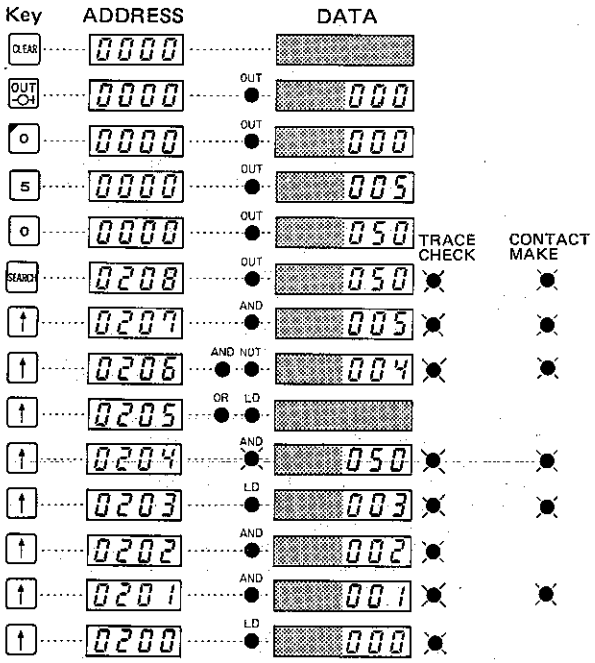
- **Operating procedure**

In the circuit for exercise shown on the right, the procedure to check the operating state of from (050) to —||— 000 in the programming sequence is shown below.



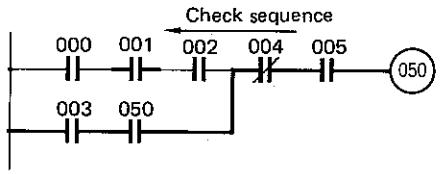
NOTE: The zero key marked [0] may or may not be depressed.

- **Display**



NOTES:
1. The above example shows the case where relays 001, 003, 005 and 050 are in the ON state and relays 000, 002 and 004 are in the OFF state.
2. In the circuit shown on the upper right, it is clear that 050 is caused to turn on by the circuit shown by the bold line.

- **Circuit for exercise and programming examples**



Address	OP	Data
200	LD	000
201	AND	001
202	AND	002
203	LD	003
204	AND	050

Address	OP	Data
205	OR-LD	
206	AND-NOT	004
207	AND	005
208	OUT	050
209	END	

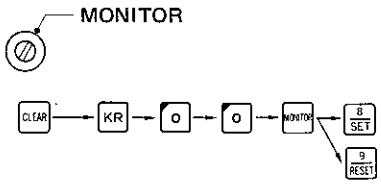
NOTES:
1. The following three methods of trace check are available.
   - Check starting from address 0000
     CLEAR → ↓ ..... ↑
   - Check starting from an OUT instruction.
     Refer to the foregoing operating procedure.
   - Check starting from an END instruction
     CLEAR → END → SEARCH → ↑ ..... ↑
     In general, an OUT instruction is first searched, and then the continuity of that block is checked according to the programming sequence.
2. No trace check is allowed after the search of an instruction other than OUT, OUT-NOT, OUT-SR, OUT-NOT-SR, OUT-KR, OUT-NOT-KR, TIM, CNT, SR, KR and END or after the setting of an address within a program except the starting address. (In this case, a beep sound is generated.)
3. The "CONTACT MAKE" indicator illuminates when continuity exists and goes out when no continuity exists. This indicator also goes out at an address where AND-LD, OR-LD, the set value of a timer or counter, IL, ILC, JMP, JME, SR, or END instruction has been set.
4. A beep sound is generated upon depression of the ↓ key after the address number has reached "2047." A beep sound is also generated upon depression of the ↑ key when the address number is "0000."

3.4.10 Forced set/reset operation

This operation is to set or reset by force the operating state of each latching relay, the operating state of each SR bit, or the present value of each timer or counter during the execution of a program. In this forced set/reset operation, the operating state of a relay is caused to be set or reset only the instant the SET or RESET key is depressed, and subsequent circuit operation is the same as originally programmed.

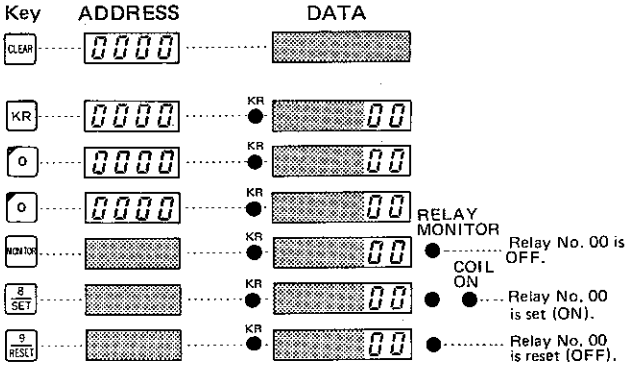
■ SET/RESET OPERATION OF THE LATCHING RELAY

- **Operating procedure**



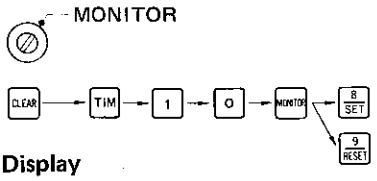
NOTE: The zero key marked [0] may or may not be depressed.

- **Display**

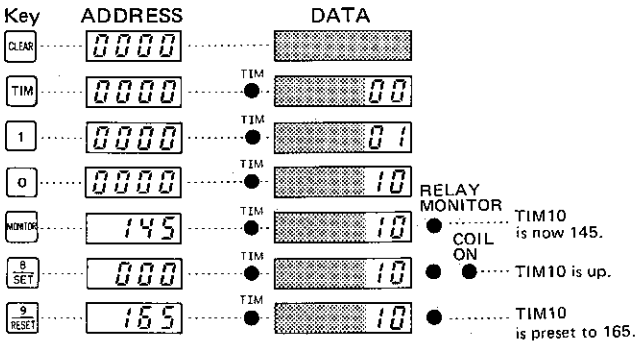


■ SET/RESET OPERATION OF THE PRESENT VALUE OF TIMER AND COUNTER

- **Operating procedure**

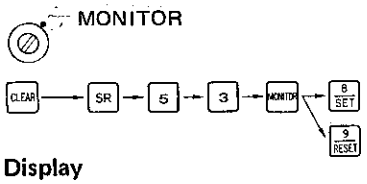


- **Display**

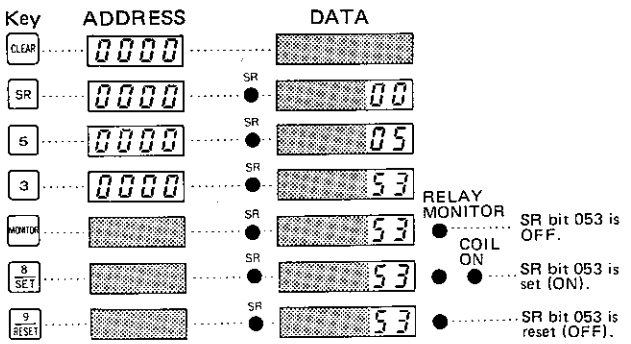


■ SET/RESET OPERATION OF THE SHIFT REGISTER

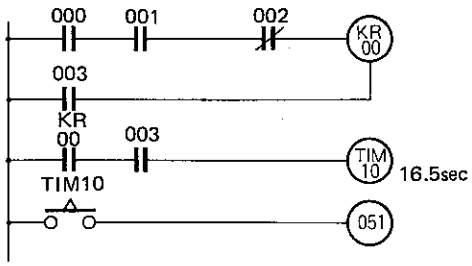
- **Operating procedure**



- **Display**



- **Circuit for exercise and programming example**



Address	OP	Data
0200	LD	000
0201	AND	001
0202	AND-NOT	002
0203	LD	003
0204	KR	00
0205	LD-KR	00

Address	OP	Data
0206	AND	003
0207	TIM	10
0208		165
0209	LD-TIM	10
0210	OUT	051
0211	END	

NOTES:

1. Forced set/reset of the operating state of a latching relay.
   When the SET key is depressed, the operating state of the specified relay number is forcedly turned ON and the "COIL ON" indicator illuminates. When the RESET key is depressed, the operating state of the specified relay numer is forcedly turned OFF and the "COIL ON" indicator goes out.
2. Forced set/reset of the present value of a timer or counter.
   When the SET key is depressed, the present value of the specified timer or counter number is forcedly cleared to zero and the "COIL ON" indicator illuminates.
   When the RESET key is depressed, the present value of the specified timer or counter number is forcedly returned to the preset value and the "COIL ON" indicator goes out.
3. Forced set/reset of the operating state of an SR bit.
   When the SET key is depressed, the operating state of the specified bit number is forcedly turned ON and the "COIL ON" indicator illuminates.
   When the RESET key is depressed, the operating state of the specified bit number is forcedly turned OFF and the "COIL ON" indicator goes out.
4. The forced set/reset function is applicable to only latching relays, timers/counters and shift registers.
5. When the SET or RESET key is depressed in any of the following cases, a beep sound is generated to alert the operator.
   ① In the CASSETTE, PROM-WRITER or RUN mode
   ② During other than the monitoring operation in the MONITOR mode
   ③ While a relay other than latching relay, timer/counter and shift register is being monitored.
   Check for the proper operating procedure.

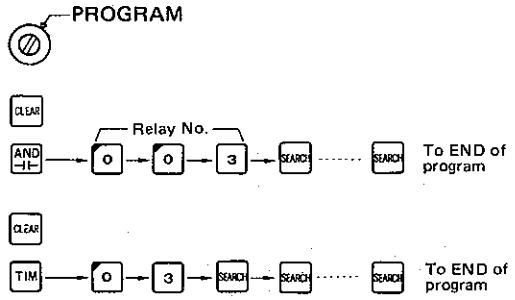
3.4.11 Instruction search operation

When a circuit change is to be made in a program simulation or test run, this operation allows an address where an instruction or relay number has been written in a program to be searched.

■ SEARCH OPERATION OF INSTRUCTION WORD

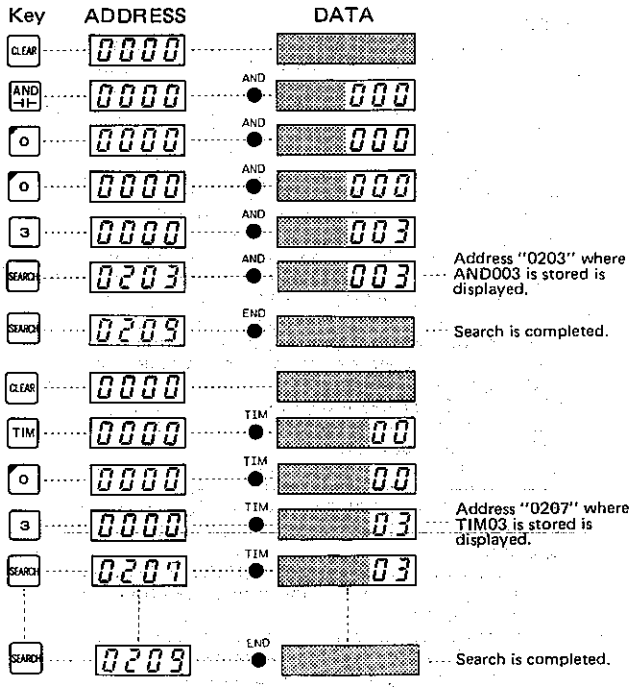
- **Operating procedure**

Referring to the circuit for exercise and programming example shown below, an example of searching 003 and TIM 03 instructions is explained here.



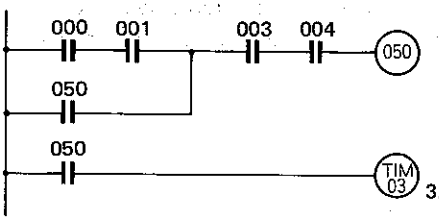
NOTE: The zero key marked 0 may or may not be depressed.

- **Display**



NOTE: The zero key marked 0 may or may not be depressed.

- **Circuit for exercise and programming example**



Address	OP	Data
0200	LD	000
0201	AND	001
0202	OR	050
0203	AND	003
0204	AND	004

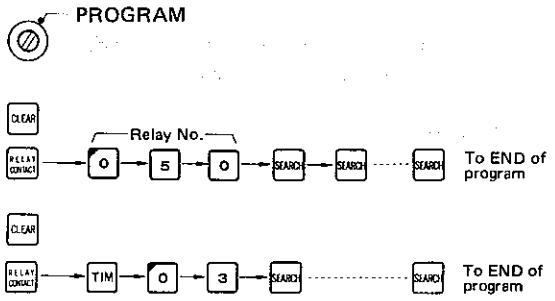
Address	OP	Data
0205	OUT	050
0206	LD	050
0207	TIM	03
0208		35
0209	END	

NOTES:
1. When the SEARCH key is depressed after entering an instruction, the first address where the instruction is stored is displayed. Continued depression of the SEARCH key causes all the addresses containing this instruction to be searched until the END instruction is encountered.
2. When the set value of a TIM, CNT, SR, or TCM instruction is to be searched, the TIM, CNT, SR or TCM instruction must be searched before depressing the ↓ key. (The set value cannot be called directly.)

■ SEARCH OPERATION OF RELAY NUMBER

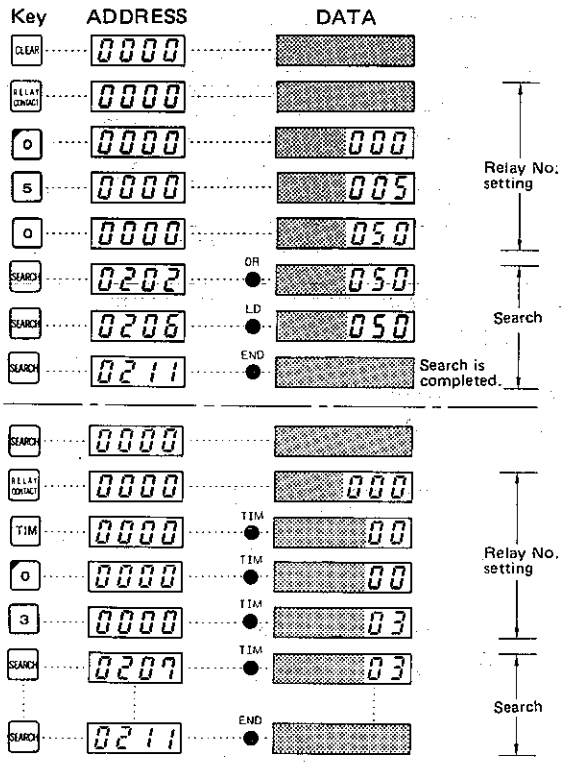
Referring to the circuit for exercise and programming example shown below, an example of searching 050 and TIM03 throughout all addresses is explained here.

- **Operating procedure**

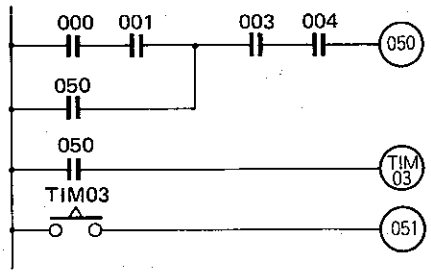


NOTE: The zero key marked 0 may or may not be depressed.

- **Display**



- **Circuit for exercise and programming example**



Address	OP	Data
0200	LD	000
0201	AND	001
0202	OR	050
0203	AND	003
0204	AND	004
0205	OUT	050

Address	OP	Data
0206	LD	050
0207	TIM	03
0208		35
0209	LD·TIM	03
0210	OUT	051
0211	END	

NOTES:

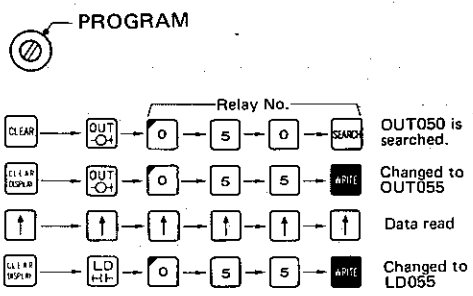
1. Depress the RELAY CONTACT key, enter the relay number (also depress the OP key in case of a TIM, CNT, SR, or KR instruction), and depress the SEARCH key respectively until the last address of a program.
   The CPU stops at each pertinent address where the relay number being searched is located.
   In other words, the relay number search operation is executed from the address being presently displayed to the address when an END instruction is located or to the last address.
   Accordingly, if another relay number is to be searched continuously, depress the CLEAR key once.
2. In this operation, the set value of a TIM, CNT, or SR instruction and the OFF time set value of a TCM instruction cannot be searched.

3.4.12 Contact (coil) number change operation

This operation is to change the contact (or coil) number in a program due to a circuit modification.

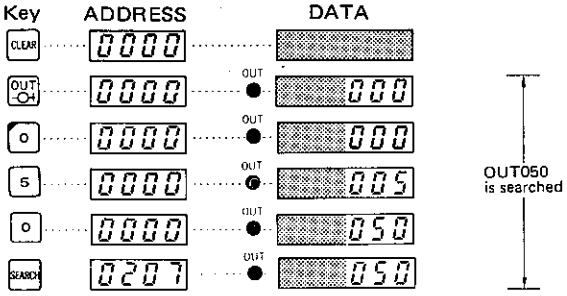
- **Operating procedure**

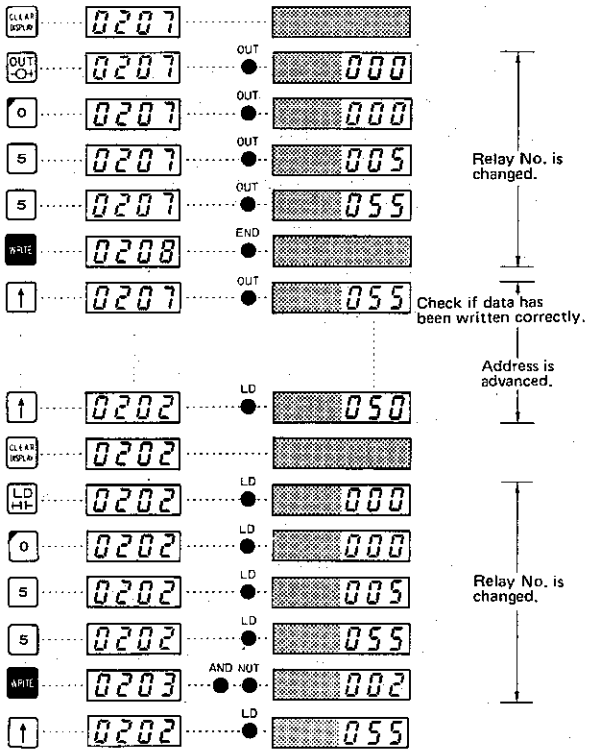
  Referring to the circuit for exercise and programming example shown on the right, an example of changing output relay No. 050 to 055 is explained here.



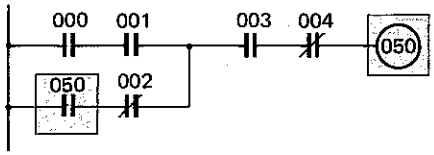
NOTE: The zero key marked [0] may or may not be depressed.

- **Display**





- **Circuit for exercise and programming example**



Address	OP	Data
0200	LD	000
0201	AND	001
0202	LD	050
0203	AND·NOT	002
0204	OR·LD	

Address	OP	Data
0205	AND	003
0206	AND·NOT	004
0207	OUT	050
0208	END	

NOTES:

1. After an OUT instruction has been searched, depress the [↑] or [↓] key continuously to decrement the address number until the address where the contact (coil) number is to be changed. The instruction to be changed at an intended address may be searched directly. However, the same instruction may in some cases be stored in other memory addresses of the same program. Therefore, it is necessary to check instructions before and after the intended address. Since no two OUT instructions with an identical relay number exist in one program, the instruction to be changed can be found easily and quickly by first searching the OUT instruction and then searching before and after the OUT instruction.
2. When changing an instruction, the contact (coil) number setting is also required.
3. When a TIM, CNT, SR, TCM or STEP No. instruction is changed to another instruction, the set value of the instruction will be deleted from memory.
   All the address numbers after the change of a TIM, CNT, SR, or STEP No. to another instruction will be decremented by 1. With a TCM instruction, however, all the address numbers will be decremented by 3.

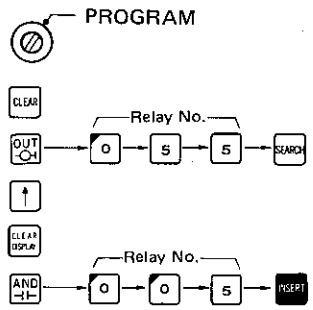
4. When a TIM, CNT, SR, TCM, or STEP No. instruction is changed from another instruction, an address in which the set value is to be entered will be automatically secured and all the address numbers after the TIM, CNT, SR, or STEP No. will be incremented by 1. With the TCM instruction, all the address numbers will be incremented by 3. In this case, the "PROGRAM OVER" indicator will illuminate unless the last address has space for 1 or 3 words, respectively, prohibiting the instruction from being written into memory.
5. When an OUT-TIM, CNT, SR, KR, OUT-NOT, OUT-SR, OUT-NOT-SR, OUT-KR, or OUT-NOT-KR instruction is to be changed to another instruction, also check the circuit related to the instruction.
6. In the above operating procedure the CLEAR DISPLAY key may be omitted from key entry.
7. After the contact (coil) number has been changed, be sure to perform the Program Check operation (CLEAR → SHIFT) to confirm that the program is free from any programming error.
8. A beep sound will be generated upon depression of the ↑ after the address number has reached "2047." A beep sound will also be generated upon depression of the ↑ key when the address number is "0000."

3.4.13 Contact (coil) addition operation

This operation is employed when the contact (or coil) number is to be added due to a circuit modification.

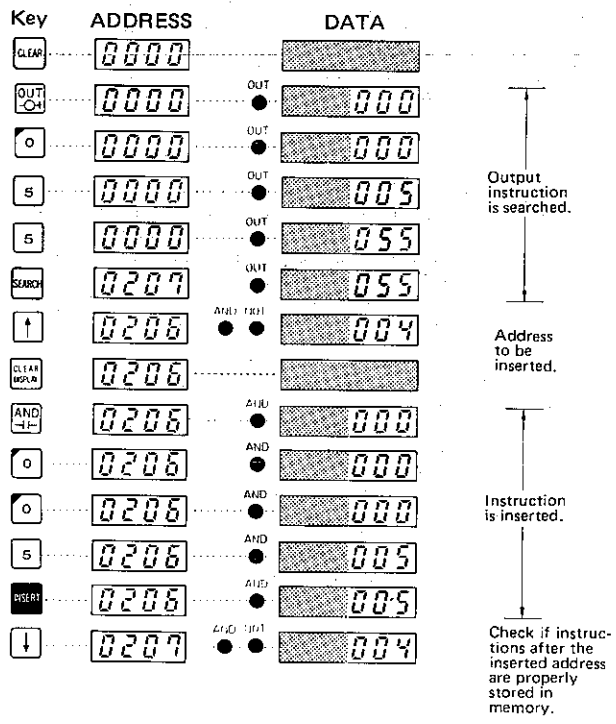
- **Operating procedure**

In the following, the procedure of adding 005 between 003 and 004 is shown.



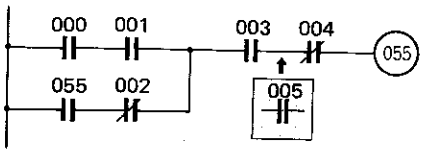
NOTE: The zero key marked 0 may or may not be depressed.

- **Display**



NOTE: The zero key marked 0 may or may not be depressed.

- **Circuit for exercise and programming example**



Before insertion

Address	OP	Data
0200	LD	000
0201	AND	001
0202	LD	055
0203	AND-NOT	002
0204	OR-LD	

Address	OP	Data
0205	AND	003
0206	AND-NOT	004
0207	OUT	055
0208	END	

After insertion

Address	OP	Data
0200	LD	000
0201	AND	001
0202	LD	055
0203	AND-NOT	002
0204	OR-LD	

Address	OP	Data
0205	AND	003
0206	AND	005
0207	AND-NOT	004
0208	OUT	055
0209	END	

NOTES:

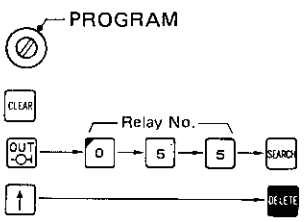
1. Search an OUT instruction, depress the ↑ key repetitively to advance the program up to the address where the instruction is to be inserted. Next, depress the CLEAR DISPLAY key, enter the instruction to be inserted and then depress the INSERT key. The address number after the inserted instruction will automatically be incremented by 1.
2. When a TIM, CNT, SR, TCM or STEP No. instruction is inserted, the address where the set value of the instruction is to be entered will be automatically secured.
3. If a "Program Over" condition occurs as a result of the instruction insertion, the "PROGRAM OVER" indicator illuminates and a beep sound is generated to alert the operator.
4. If an attempt is made to insert an instruction into the address where the set value of a timer or counter has been set, a beep sound is generated to signal the operator that the instruction cannot be inserted.
5. In other than the PROGRAM mode, no instruction can be inserted.
6. After the instruction to be inserted has been entered, depression of the INSERT key two or more times in succession will be ignored and no instruction can be entered.
7. After the insertion of the instruction, confirm instructions before and after the inserted address.
8. After the contact (coil) number has been inserted, be sure to perform the Program Check operation (CLEAR → SHIFT) to confirm that the program is free from any programming error.

3.4.14 Contact (coil) deletion operation

This operation is to delete contact (or coil) number(s) from a program due to a circuit modification.

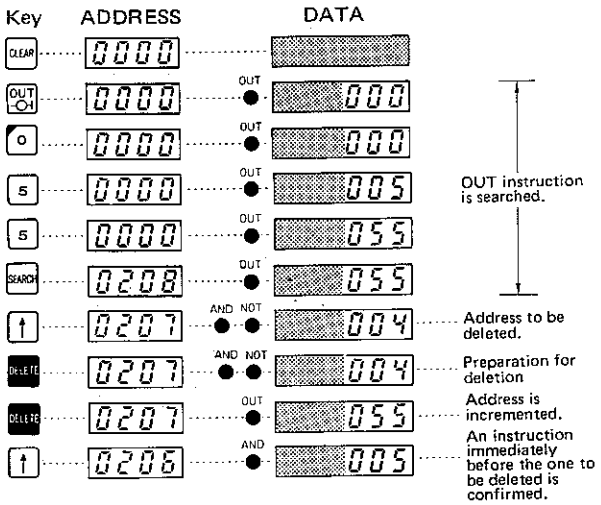
- **Operating procedure**

Referring to the circuit for exercise shown below, an example of deleting 004 is explained.

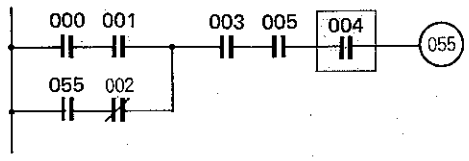


NOTE: The zero key marked 0 may or may not be depressed.

- **Display**



- **Circuit for exercise and programming example**



Before deletion

Address	OP	Data
0200	LD	000
0201	AND	001
0202	LD	055
0203	AND-NOT	002
0204	OR-LD	

Address	OP	Data
0205	AND	003
0206	AND	005
0207	AND-NOT	004
0208	OUT	055
0209	END	

After deletion

Address	OP	Data
0200	LD	000
0201	AND	001
0202	LD	055
0203	AND-NOT	002
0204	OR-LD	

Address	OP	Data
0205	AND	003
0206	AND	005
0207	OUT	055
0208	END	
0209		

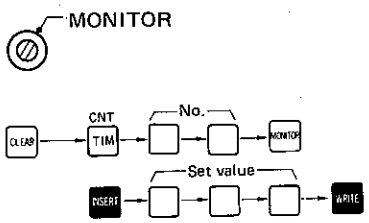
NOTES:

1. Search an OUT instruction, depress the [↑] key to advance the program up to the address where the instruction to be deleted is located, and depress the DELETE key twice in succession. All the address numbers after the deleted instruction will automatically be decremented by 1.
   The reason for depressing the DELETE key twice is to prevent an instruction from being deleted accidentally due to an erroneous key operation. The first depression of the key causes a beep sound to be generated to signal the preparation for an instruction deletion. The second and each subsequent depression of the key cause instructions to be deleted one by one.
2. When a TIM, CNT, SR, or TCM instruction is deleted, the address where the set value of the instruction is located will also be deleted automatically. Only the set value of a TIM, CNT, SR or TCM instruction cannot be deleted. (A beep sound will be generated if an attempt is made to do so.)
3. After the instruction has been deleted, confirm instructions before and after the deleted address.
4. After the deletion of the instruction, be sure to execute the Program Check operation ([CLR] → [SHIFT]). Particularly, the program check is mandatory when such an instruction as LD, OUT, TIM, or CNT is deleted.

3.4.15 Set value change operation of timer and counter

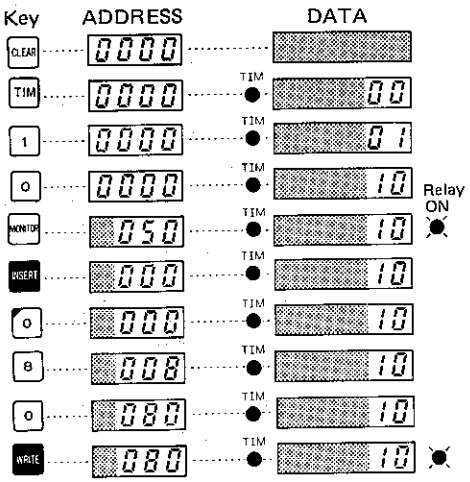
This operation is to change the set value of a timer or counter during the execution of a ladder diagram program. The set value changed in this operation will become effective only when the timer or counter operates next time.

- **Operating procedure**



- **Display**

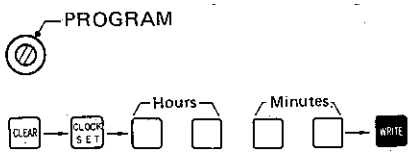
(Example) The set value is changed from 5sec to 8sec.



3.4.16 Time setting operation of the 24-hour clock

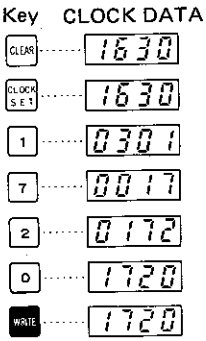
This operation is to correct or advance the time indicated by the 24-hour clock.

- **Operating procedure**



- **Display**

(Example) The time is changed from 16:30 to 17:20 hours.



4. Step Advance Type Programming

4.1 Assignment of Relay Numbers

Relay numbers correspond to the data memory areas and the operation (ON/OFF state) of each relay is stored in the corresponding memory area.

The method of assigning relay numbers used for the step advance programming is as follows.

4.1.1 List of relay numbers

- **Type SCY-P5R10E**

Name	No. of points	Symbol	Relay number									
Input relay	48	–	000	001	002	003	004	005	006	007	008	009
			010	011	012	013	014	015	016	017	018	019
			020	021	022	023	024	025	026	027	028	029
			030	031	032	033	034	035	036	037	038	039
			040	041	042	043	044	045	046	047		
Output relay	48	–	050	051	052	053	054	055	056	057	When STEP CON-0 is used.	
			058	059	060	061	062	063	064	065		
			066	067	068	069	070	071	072	073	When STEP CON-1 is used.	
			074	075	076	077	078	079	080	081		
			082	083	084	085	086	087	088	089	When STEP CON-2 is used.	
			090	091	092	093	094	095	096	097		
Internal auxiliary relay	152	–									098	099
			100	101	102	103	104	105	106	107	108	109
			110	111	112	113	114	115	116	117	118	119
			120	121	122	123	124	125	126	127	128	129
			130	131	132	133	134	135	136	137	138	139
			140	141	142	143	144	145	146	147	148	149
			150	151	152	153	154	155	156	157	158	159
			160	161	162	163	164	165	166	167	168	169
			170	171	172	173	174	175	176	177	178	179
			180	181	182	183	184	185	186	187	188	189
			190	191	192	193	194	195	196	197	198	199
			200	201	202	203	204	205	206	207	208	209
			210	211	212	213	214	215	216	217	218	219
			220	221	222	223	224	225	226	227	228	229
			230	231	232	233	234	235	236	237	238	239
			240	241	242	243	244	245	246	247	248	249

Name	No. of points	Relay number	Description
Special auxiliary relay	6	250	0.1sec clock
		251	1sec clock
		252	1min clock
		253	Turns ON when the battery is abnormal.
		254	Turns ON when the 24-hour clock is abnormal.
		255	Normally ON

NOTE: With the SCY-P5R10E, relay numbers other than above cannot be used.

- **Type SCY-P5R30E**

Name	No. of points	Symbol	Relay number									
Input relay	32	—	000	001	002	003	004	005	006	007	008	009
			010	012	012	013	014	015	016	017	018	019
			020	021	022	023	024	025	026	027	028	029
			030	031								
Output relay	24*	—	050	051	052	053	054	055	056	057	When STEP CON-0 is used.	
			058	059	060	061	062	063	064	065		
			066	067	068	069	070	071	072	073	When STEP CON-1 is used.	
			074	075	076	077	078	079	080	081		
Internal auxiliary relay	168	—			082	083	084	085	086	087	088	089
			090	091	092	093	094	095	096	097	098	099
			100	101	102	103	104	105	106	107	108	109
			110	111	112	113	114	115	116	117	118	119
			120	121	122	123	124	125	126	127	128	129
			130	131	132	133	134	135	136	137	138	139
			140	141	142	143	144	145	146	147	148	149
			150	151	152	153	154	155	156	157	158	159
			160	161	162	163	164	165	166	167	168	169
			170	171	172	173	174	175	176	177	178	179
			180	181	182	183	184	185	186	187	188	189
			190	191	192	193	194	195	196	197	198	199
			200	201	202	203	204	205	206	207	208	209
			210	211	212	213	214	215	216	217	218	219
			220	221	222	223	224	225	226	227	228	229
			230	231	232	233	234	235	236	237	238	239
			240	241	242	243	244	245	246	247	248	249

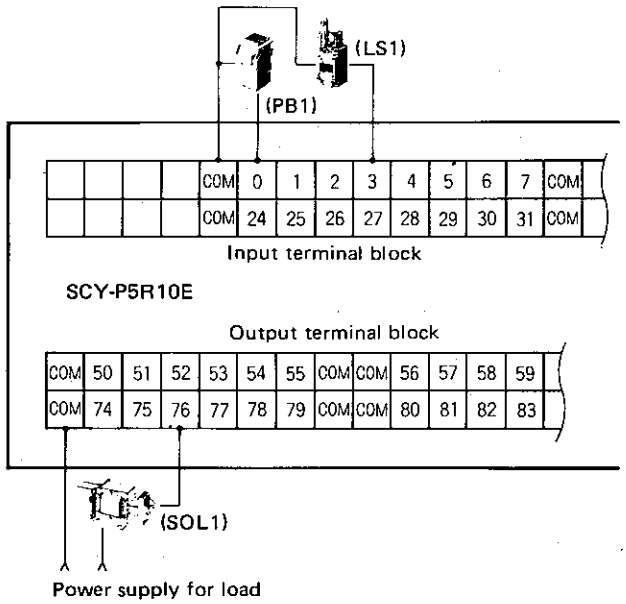
NOTE: * The SCY-P5R30E is provided with 24 output relays (050 thru 073). Relay Nos. 074 thru 081 are the auxiliary relays which can be turned ON or OFF within the step controller group 1 program.

Name	No. of points	Relay number	Description
Special auxiliary relay	6	250	0.1sec clock
		251	1sec clock
		252	1min clock
		253	Turns ON when the battery is abnormal.
		254	Turns ON when the 24-hour clock is abnormal.
		255	Normally ON

NOTE: With the SCY-P5R30E, relay numbers other than above cannot be used.

4.1.2 Determination of I/O relay numbers

1. In a sequence circuit diagram which is generally known, a sequence circuit is drawn with input/output devices included and I/O device symbols and relay numbers are arbitrarily determined. However, since the SYSMAC-P5R cannot recognize such arbitrary I/O device symbols and relay numbers, it is necessary to determine the I/O terminals to which I/O devices are to be connected.
2. The SYSMAC-P5R requires the relay numbers corresponding to the I/O devices for programming. The relay numbers are determined by the locations (I/O terminals) of I/O terminal blocks to which the I/O devices are connected. Each of these relay numbers must be used for the step advance type programming.



NOTES:
1. Output relay coil numbers may be used in duplication within the same step controller.
2. For Type SCY-P5R10E, relay numbers 050 through 097 can be used as output relays. For SCY-P5R30E, relay numbers 050 through 073 can be used for the same purpose.
3. For Type SCY-P5R10E, relay numbers 000 through 255 can be used to set input conditions. For Type SCY-P5R30E, relay numbers 000 through 031 and 050 through 255 can be used for the same purpose. The number of input conditions is not limited.

4.1.3 Determination of internal auxiliary relay numbers

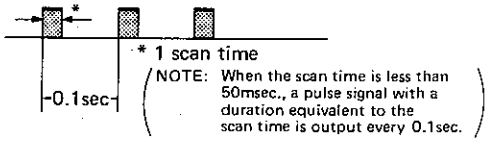
The SYSMAC-P5R has a number of internal auxiliary relays which are used for internal data transfer in sequence circuits. They are independent of I/O devices in sequence. Since the internal auxiliary relays are the data memories incorporated in the CPU, no wiring to the I/O terminals is required. (In other words, they cannot be used as contact outputs.)

NOTES: 1. Internal auxiliary relays cannot be used as the output relays. However, they can be used to set input conditions. The number of input conditions is not limited.
2. Relay numbers may not necessarily be assigned consecutively.

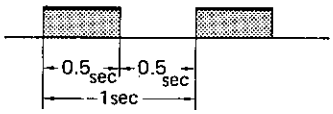
4.1.4 Determination of special auxiliary relay numbers

6 special auxiliary relays are provided. These relays are sort of internal auxiliary relays which operate and release according to the internal conditions controlled by hardware and are independent of the I/O devices in sequence.

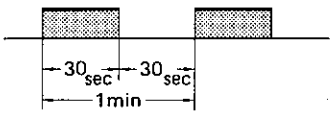
250: This relay is used to generate 0.1sec clock. When used in conjunction with a counter, it functions as a timer for memory retention during a power failure.



251: This relay is used to generate 1sec clock. When used in conjunction with a counter, it functions as a timer for memory retention during a power failure. The relay output can also be used as a flicker signal.



252: This relay is used to generate 1min clock. When used in conjunction with a counter, it functions as a timer for memory retention during a power failure.



253: This relay operates when a battery failure occurs and releases when the battery is returned to normal. When this relay operates, the BATTERY FAILURE indicator on the front panel of the CPU illuminates. If the BAT FAULT signal is desired to be transmitted externally, prepare and program a circuit using the contacts of this relay.
(Refer to paragraph 3.3.2 Applied Programs.)

254: This relay operates when a clock failure occurs and releases when the 24-hour clock is returned to normal. To release this relay, push the CLEAR key. If the CLOCK FAULT signal is desired to be transmitted externally, prepare and program a circuit using the contacts of this relay.
(Refer to paragraph 3.3.2 Applied Programs.)

255: This relay is normally in the ON state.

4.2 Instruction Words

4.2.1 List of instructions

- **SCY-P5R10E**

Title	OP	DATA-1	DATA-2	Remarks	Word length
STEP CONTROLLER	STEP CON	–	Step controller group designation (0 ~ 2)	Specifies the group number of a step advance type program.	1W
STEP END	STEP END	–	–	Indicates the end of a step advance type program for the specified group number.	7W
MANUAL END	MANU END	–	–	Indicates the end of a ladder diagram program for manual operation of a step controller.	1W
LOGICAL AND	AND	Relay number (000 ~ 047, 050 ~ 255)	Relay number (000 ~ 047, 050 ~ 255)	When the relay Nos. specified by DATA-1 and DATA-2 are ANDed, the program proceeds to the next step if the result of the AND operation is "1."	7W
LOGICAL OR	OR	Relay number (000 ~ 047, 050 ~ 255)	Relay number (000 ~ 047, 050 ~ 255)	When the relay Nos. specified by DATA-1 and DATA-2 are ORed, the program proceeds to the next step if the result of the OR operation is "1."	7W
TIMER	TIM	Set count value (000 ~ 255)	Clock input (000 ~ 002)	When the clock input specified by DATA-2 is counted and reaches the set time value specified by DATA-1, the program proceeds to the next step.	7W
COUNTER	CNT	Set count value (000 ~ 255)	Count input (000 ~ 047, 050 ~ 255)	When the count input specified by DATA-2 is counted and reaches the set count value specified by DATA-1, the program proceeds to the next step.	7W
CONDITIONAL JUMP	CJP	Step to which program jumps' (001 ~ 099)	Relay number (000 ~ 047, 050 ~ 255)	When the condition of the relay No. specified by DATA-2 is YES, the program jumps to the step No. specified by DATA-1. If NO, it proceeds to the next step.	7W

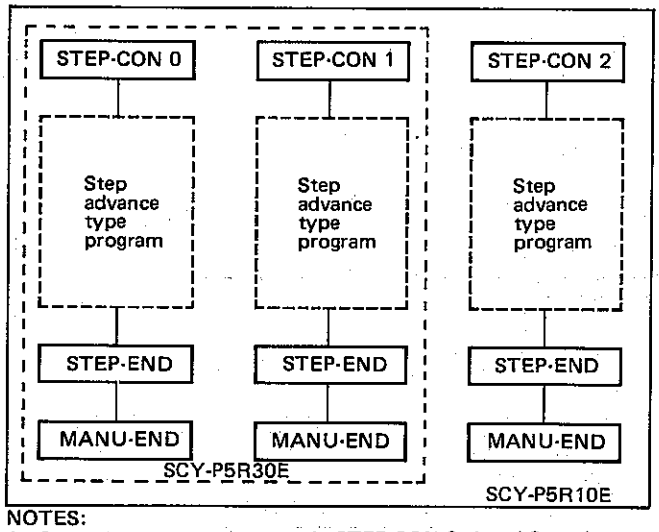
- **SCY-P5R30E**

Title	OP	DATA-1	DATA-2	Remarks	Word length
STEP CONTROLLER	STEP CON	–	Step controller group designation (0 ~ 1)	Specifies the group number of a step advance type program.	1W
STEP END	STEP END	–	–	Indicates the end of a step advance type program for the specified group number.	7W
MANUAL END	MANU END	–	–	Indicates the end of a ladder diagram program for manual operation of a step controller.	1W
LOGICAL AND	AND	Relay number (000 ~ 031, 050 ~ 255)	Relay number (000 ~ 031, 050 ~ 255)	When the relay Nos. specified by DATA-1 and DATA-2 are ANDed, the program proceeds to the next step if the result of the AND operation is "1."	7W
LOGICAL OR	OR	Relay number (000 ~ 031, 050 ~ 255)	Relay number (000 ~ 031, 050 ~ 255)	When the relay Nos. specified by DATA-1 and DATA-2 are ORed, the program proceeds to the next step if the result of the OR operation is "1."	7W
TIMER	TIM	Set count value (000 ~ 031, 050 ~ 255)	Clock input (000 ~ 031, 050 ~ 255)	When the clock input specified by DATA-2 is counted and reaches the set time value specified by DATA-1, the program proceeds to the next step.	7W
COUNTER	CNT	Set count value (000 ~ 031, 050 ~ 255)	Count input (000 ~ 031, 050 ~ 255)	When the count input specified by DATA-2 is counted and reaches the set count value specified by DATA-1, the program proceeds to the next step.	7W
CONDITIONAL JUMP	CJP	Set to which program jumps (001 ~ 099)	Relay number (000 ~ 031, 050 ~ 255)	When the condition of the relay No. specified by DATA-2 is YES, the program jumps to the step No. specified by DATA-1. If NO, it proceeds to the next step.	7W

4.2.2 Explanation of instruction words

■ STEP CONTROLLER/STEP END (STEP CON/STEP END) INSTRUCTIONS

These instructions are used to specify the group number of a step advance type program and to indicate the end of a step advance type program for the specified group number, respectively.

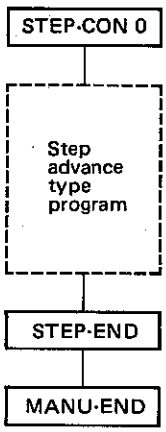


NOTES:
1. Step advance type programs in STEP CON 0, 1 and 2 can be operated concurrently. STEP CON 0, 1 and 2 may not necessarily be used consecutively.
2. Immediately before each STEP CON instruction, the conditions that cause the entire step advance type program to operate (i.e., output inhibit, forced advance, auto advance, auto/manual and reset) are always required.

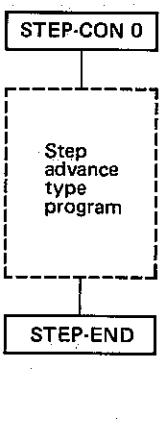
■ MANUAL END (MANU END) INSTRUCTION

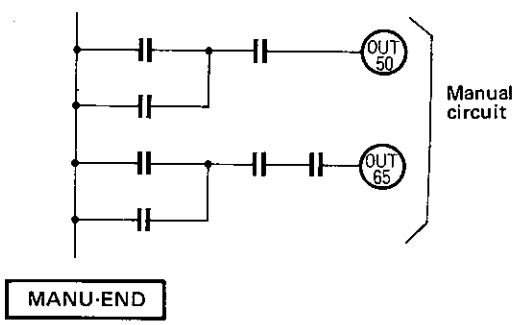
To operate any of the three step advance controllers manually, program a manual circuit after the STEP END instruction using the ladder diagram programming method, and then enter the MANU END instruction. Where a manual circuit is not required, program only the MANU END instruction.

- **When manual circuit is not required.**



- **When manual circuit is required.**





■ LOGICAL AND INSTRUCTION

OP	DATA-1	DATA-2
AND	Relay number • 000 ~ 047, 050 ~ 255 (SCY-P5R10E) • 000 ~ 031, 050 ~ 255 (SCY-P5R30E)	Relay number • 000 ~ 047, 050 ~ 255 (SCY-P5R10E) • 000 ~ 031, 050 ~ 255 (SCY-P5R30E)

- **Function**
  1. The relay numbers specified by DATA-1 and DATA-2 are ANDed and if the result of the AND operation is "1," the program proceeds to the next step.
  2. Before setting each relay number, the logical state of the relay can be inverted by depressing the NOT key.
  3. With this instruction, output setting is possible.

■ LOGICAL OR INSTRUCTION

OP	DATA-1	DATA-2
OR	Relay number • 000 ~ 047, 050 ~ 255 (SCY-P5R10E) • 000 ~ 031, 050 ~ 255 (SCY-P5R30E)	Relay number • 000 ~ 047, 050 ~ 255 (SCY-P5R10E) • 000 ~ 031, 050 ~ 255 (SCY-P5R30E)

- **Function**
  1. The relay numbers specified by DATA-1 and DATA-2 are ORed and if the result of the OR operation is "1," the program proceeds to the next step.
  2. Before setting each relay number, the logical state of the relay can be inverted by depressing the NOT key.
  3. With this instruction, output setting is possible.

■ TIMER (TIM) INSTRUCTION

OP	DATA-1	DATA-2
TIM	Set time value 000 ~ 255	Clock input 000 ~ 002

- **Function**
  1. The clock input specified by DATA-2 is counted and the program proceeds to the next step when the counted value reaches the set time value specified by DATA-1.
  2. Available clock inputs are as follows.
     000 → 0.1sec
     001 → 1.0sec
     002 → 1 min
  3. With this instruction, output setting is possible.
  4. When a power failure occurs, the present value of the timer is cleared from memory.

■ COUNTER (CNT) INSTRUCTION

OP	DATA-1	DATA-2
CNT	Set count value 000 ~ 255	Count input • Relay number 000 ~ 047, 050 ~ 255 (SCY-P5R10E) • Relay number 000 ~ 031, 050 ~ 255 (SCY-P5R30E)

- **Function**
  1. The count input specified by DATA-2 is counted and the program proceeds to the next step when the counted value reaches the set count value specified by DATA-1.
  2. Before setting a count input, the logical state of the counter can be inverted by depressing the NOT key.
  3. With this instruction, output setting is possible.
  4. When a power failure occurs, the present value of the counter is cleared from memory.

■ CONDITIONAL (CJP) JUMP INSTRUCTION

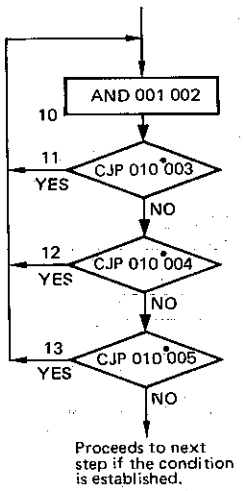
OP	DATA-1	DATA-2
CJP	Step to which program jumps 001 ~ 099	Relay number • 000 ~ 047, 050 ~ 255 (SCY-P5R10E) • 000 ~ 031, 050 ~ 255 (SCY-P5R30E)

- **Function**
  1. When the relay number specified by DATA-2 is YES, the program jumps to the step specified by DATA-1. If NO, it proceeds to the next step.
  2. Before setting each relay number, the logical state of the relay can be inverted by depressing the NOT key.
  3. With this instruction, output setting is impossible.

4.2.3 Application of instruction words

■ PROGRAMMING FOR ANDING MULTIPLE INPUTS

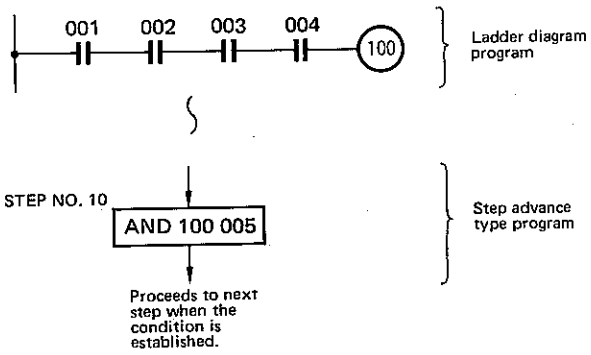
- **When AND and CJP instructions are used**



Address	Step	OP	Data	
0200 ~ 0206	10	AND	001	002
0207 ~ 0213	11	CJP	010	*003*
0214 ~ 0220	12	CJP	010	*004
0221 ~ 0227	13	CJP	010	*005

NOTES:
1. Since a CJP instruction can specify the jump-to-step at the YES decision, the instruction is used by inverting the final condition.
2. **003 indicates that the input state of 003 is inverted.

- **When AND instruction is used with ladder diagram instructions.**

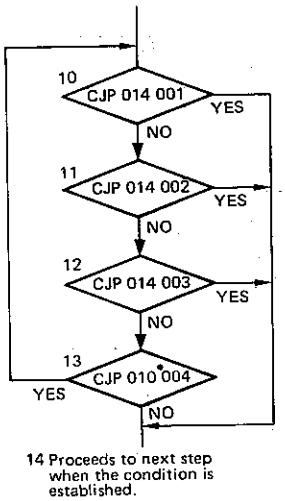


Address	Step	OP	Data	
0200		LD		001
0201		AND		002
0202		AND		003
0203		AND		004
0204		OUT		100*
⟆		⟆		
0350 ~ 0356	10	AND	100	005

NOTES:
1. When a series circuit is composed of relays and the result is output to an internal auxiliary relay, the program capacity will decrease if the decision for the auxiliary relay is made using an AND instruction.
2. * Signals between a ladder diagram program and a step advance type program must be transmitted and received through output relays or internal auxiliary relays.

■ PROGRAMMING FOR ORING MULTIPLE INPUTS

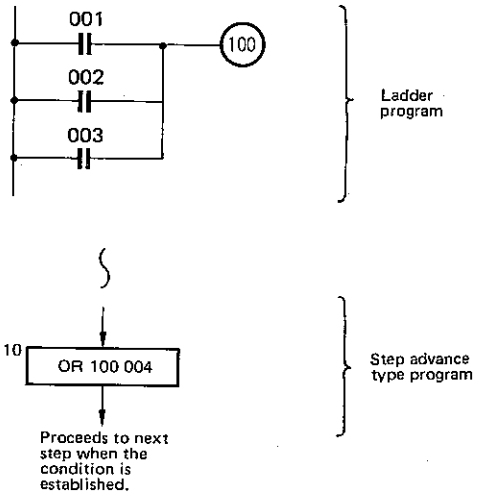
- **When CJP instructions are used.**



Address	Step	OP	Data	
0200 ~ 0206	10	CJP	014	001
0207 ~ 0213	11	CJP	014	002
0214 ~ 0220	12	CJP	014	003
0221 ~ 0227	13	CJP	010	*004*
0228 ~ 0234	14			

NOTES:
1. Since a CJP instruction can specify the jump-to-step at the YES decision, the instruction is used by inverting the final condition.
2. **004 indicates that the input state of 004 is inverted.

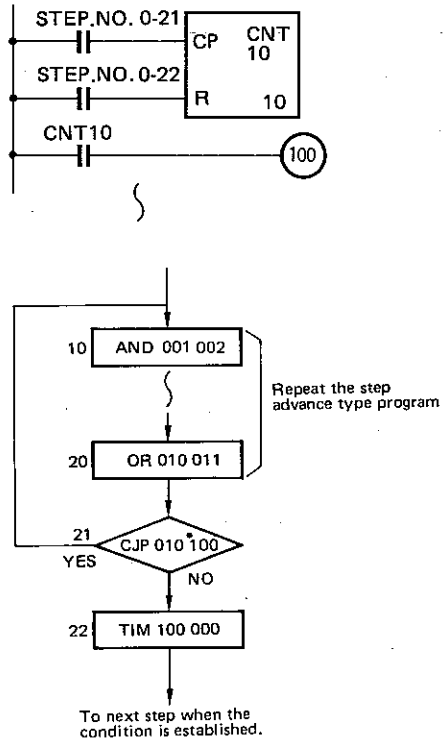
- **When OR instruction and relay circuit are used.**



Address	Step	OP	Data	
0200		LD		001
0201		OR		002
0202		OR		003
0203		OUT		100*
0350 ~ 0356	10	OR	100	004

NOTES:
1. When a parallel circuit is composed of relays and the result is output to an internal auxiliary relay, the program capacity will decrease if the decision for the auxiliary relay is made using an OR instruction.
2. *Signals between a ladder diagram and a step advance type program must be transmitted and received through output relays or internal auxiliary relays.

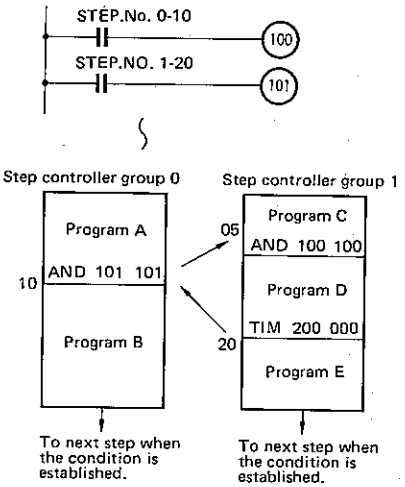
■ TO REPEAT A STEP ADVANCE TYPE PROGRAM (FOR EXAMPLE, 10 TIMES)



Address	Step	OP	Data	
0200 ~ 0201		LD, STEP NO.		021
0202 ~ 0203		LD, STEP NO.		022
0204		CNT		10
0205				010
0206		LD, CNT		10
0207		OUT		100*
0350 ~ 0356	10	AND	001	002
0420 ~ 0426	20	OR	010	011
0427 ~ 0433	21	CJP	010	*100
0434 ~ 0440	22	TIM	100	000

NOTES:
1. Develop a counter circuit using ladder diagram instructions to count the number of repetitions, output the count-up signal to an internal auxiliary relay and then make a decision on the result with a CJP instruction.
2. Signals between a ladder diagram program and a step advance type program must be transmitted and received through output relays and internal auxiliary relays.

■ TO OPERATE STEP CONTROLLERS PARALLELLY



Address	Step	OP	Data		
0200 ~ 0201		LD, STEP NO.		010	
0202		OUT		100	
0203 ~ 0204		LD, STEP NO.		120	
0205		OUT		101	
		(Program A)			Step controller group 0
0350 ~ 0356	10	AND	101	101	
		(Program B)			
		(Program C)			
0600 ~ 6506	05	AND	100	100	
		(Program D)			Step controller group 1
0705 ~ 0711	20	TIM	200	000	
		(Program E)			

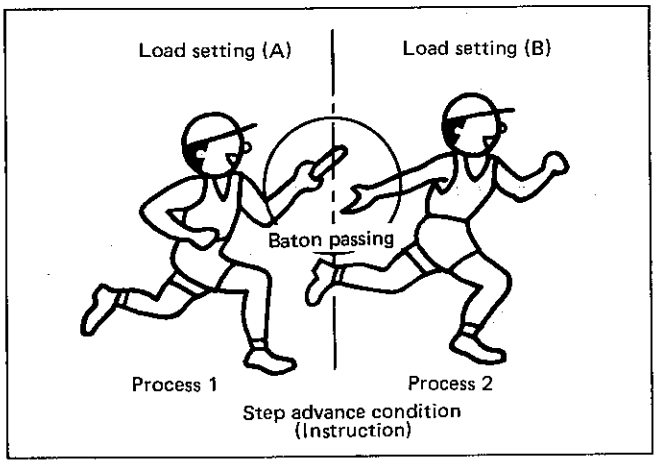
- Programs A and C operate parallelly, and then program C stops at step 05. When program A advances to step 10 and stops there, program D will start operating.
- When program D advances to step 20, programs B and E will start operating.

4.3 Programming

4.3.1 What is a step advance type programming?

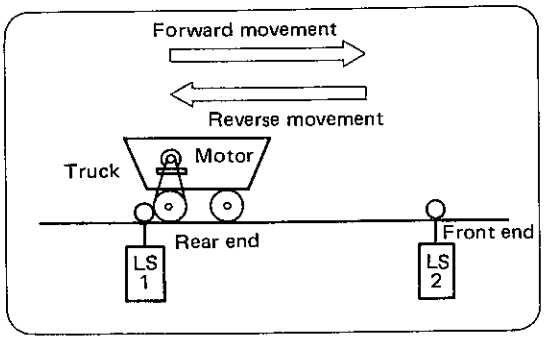
A step controller segments a process or operation according to the movements of inputs and outputs to be controlled by taking each such movement as is expressed on a timing chart. Each segment of the process or operation is called "STEP." The step controller advances the segmented steps depending on the conditions such as timer, counter, external signal, etc. It establishes both the load for each step and the conditions to advance each step.

For better understanding, if the step advance process is assumed to be a relay race, runners A and B correspond to actual loads, while the baton passing corresponds to step advance conditions. Step advance conditions are hereafter referred to as "Instructions." Since the step controller permits programming according to the movement of a controlled system (e.g., movement of a machine) without the need of sequence diagrams previously prepared by specialists such as electrical engineers, programs can be made easily by mechanical engineers and even by persons in charge at sites.

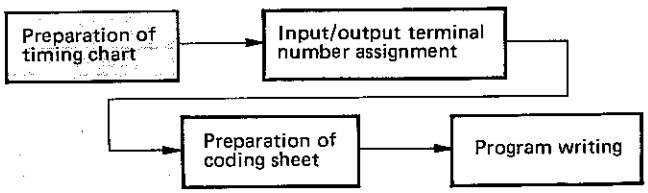


4.3.2 Programming procedure

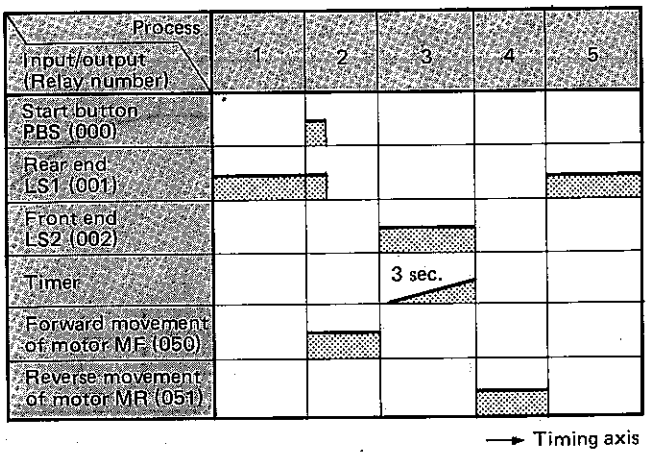
The SYSMAC-P5R has been designed to permit easy programming. After designing a control system and listing required input/output devices, prepare a program following the procedure described below. Using the following example of operation, procedures from the preparation of timing charts to practical programs are explained.

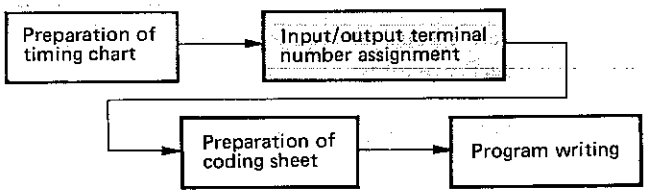


1. When start button (PBS) is depressed with LS1 in the ON state, the truck driving motor rotates in the forward direction, causing the truck to move forward.
2. When LS2 is turned on, the motor stops and at the same time the timer starts to function.
3. The motor rotates in the reverse direction after the set time has elapsed (3 sec.), causing the truck to move backward.
4. LS1 is turned ON, and then the motor stops.



Segment the operation by the sequence of each process and prepare the timing chart as shown below with the data (input) and work or load (output) expressed on the timing axis.

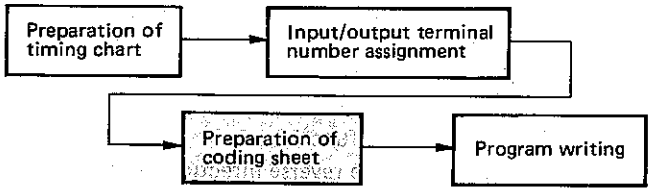




Since the SYSMAC-P5R cannot identify input/output devices by names such as sensor, motor, etc., determine the input/output terminal numbers and assign them to the respective I/O devices so that they can be recognized in programs.

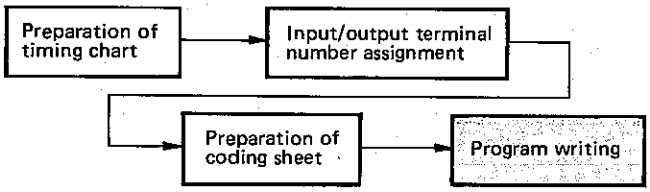
Input terminal numbers: 000 through 047
Output terminal numbers: 050 through 065
(with STEP CON 0)

Description of input/output		Terminal No.	
		Input	Output
Start button	PBS	000	
Reverse movement	LS1	001	
Forward movement	LS2	002	
Forward movement of motor	MF		050
Reverse movement of motor	MR		051



Prepare the specified coding sheet as shown below with the predetermined instruction words. Reproduce the coding sheet (blank form) attached to this manual for use in programming.

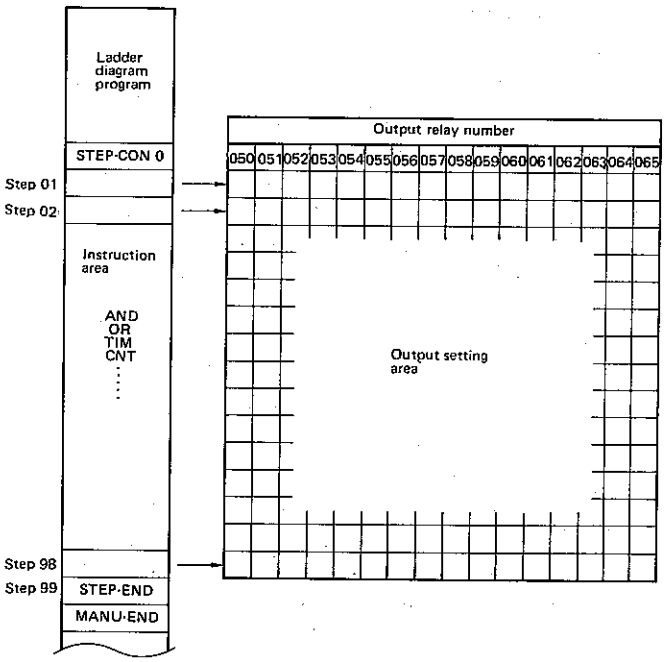
Address	STEP No.	Instruction	Data		Output				
			DATA-1	DATA-2	050	051	052	053	054
0020		STEP CON		0					
0021 ~ 0027	01	AND	000	001					
0028 ~ 0034	02	OR	002	002		ON			
0035 ~ 0041	03	TIM	030	000					
0042 ~ 0048	04	OR	001	001	ON				
0049 ~ 0055	05	STEP END							
0056									



Write a program through the program console referring to 4.4, Operating Procedure.

4.3.3 Relationship between step and output

Each step (01 ~ 99) of a step advance type program has an area to store instructions and an area to set outputs. Note that some instructions allow output setting while other instructions do not. With the instructions that allow output setting, an output turns on when it advances to the step where the output setting exists and turns off at the step where no output setting exists. With the instructions that do not allow output setting, one instruction causes the output state of the previous step to be retained, while another causes all outputs to be turned off.

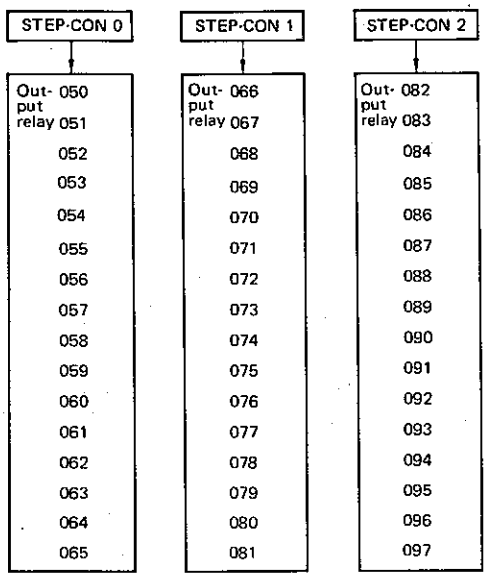


- **Instructions that allow output setting:**
  AND
  OR
  TIM
  CNT
- **Instructions that do not allow output setting:**
  CJP (causes the output state of the previous step to be retained)
  STEP END (causes all outputs to turn off)
  STEP CON
  MANU END

4.3.4 Relationship between step controller groups and outputs

- **SCY-P5R10E**

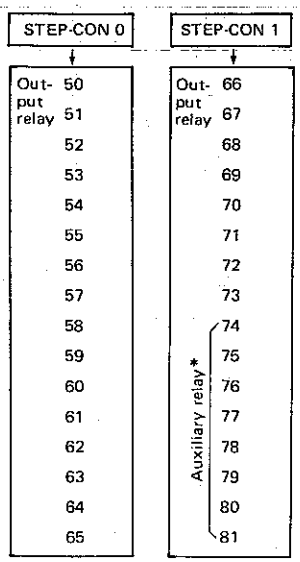
Step advance programming is possible for a maximum of 3 step controller groups to determine the outputs to be controlled by each group.



NOTES:
1. Output relays assigned to one step controller group cannot be used by any other step controller group.
2. Output relays alone can be subjected to ON/OFF control, while internal auxiliary relays and special auxiliary relays cannot. However, logical decision is possible with the AND, OR, CJP, or CNT instruction.
3. If any output relays used by each step controller group are used in a ladder diagram program, relay coil numbers will result in duplication, except when used in a manual program.

- **SCY-P5R30E**

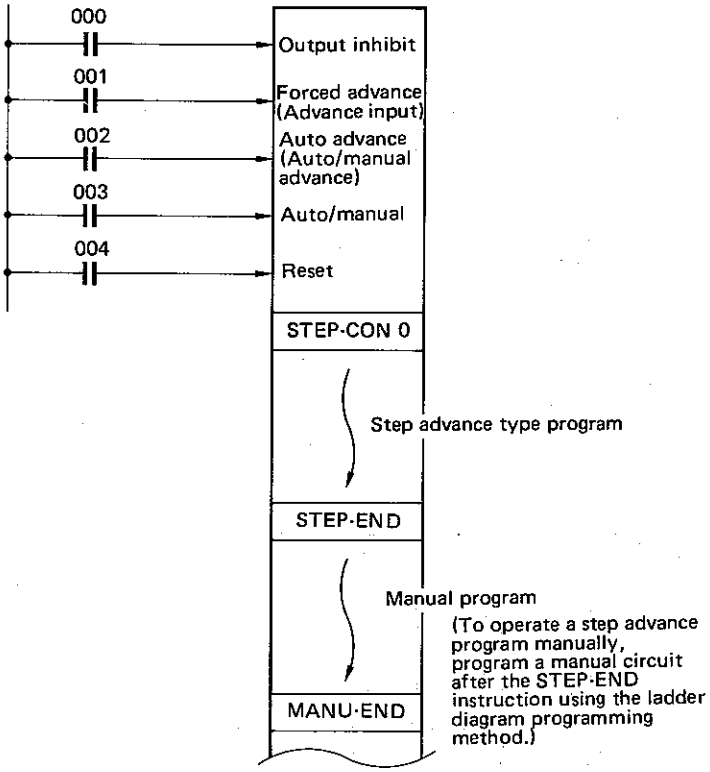
Step advance programming is possible for a maximum of 2 step controller groups to determine the outputs to be controlled by each group.



NOTES:
1. * Output relays assigned to one step controller group cannot be used by any other controller group. However, relay Nos. 74 ~ 81 within the step controller group 1 are for use as internal auxiliary relays in ladder diagram program.
2. Output relays alone can be subjected to ON/OFF control, while internal auxiliary relays and special auxiliary relays cannot. However, logical decision is possible with the AND, OR, CJP, or CNT instruction.
3. If any output relays used by each step controller group are used in a ladder diagram program, relay coil numbers will result in duplication, except when used in a manual program.

4.3.5 Operating conditions of the step controller

Immediately before programming each step controller group (STEP·CON 0 ~ 2), a program to specify the operating conditions required in controlling the group must be entered.



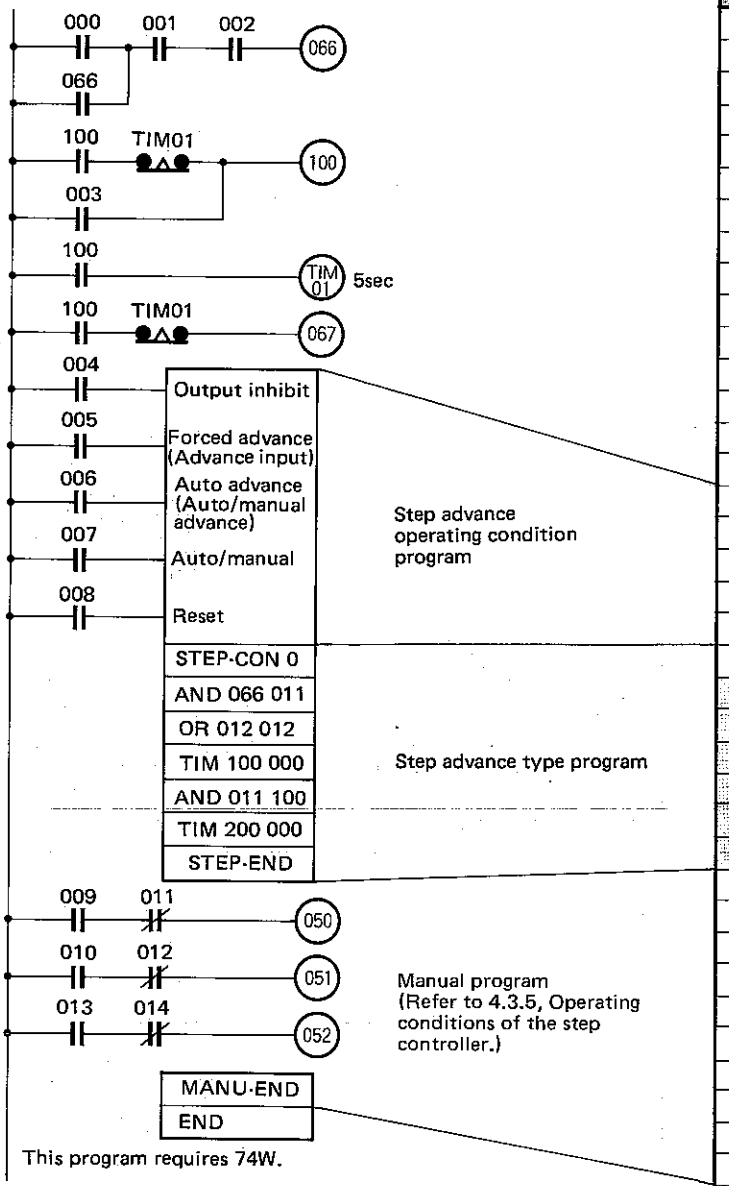
- **Operating conditions**

Conditions					Description
Output inhibit	Forced advance (Advance input)	Auto advance (Auto advance/ manual advance)	Auto/ manual	Reset	
"ON"	"—"	"—"	"ON"	"OFF"	Turns off all the outputs within the group.
"OFF"	"—"	"ON"	"ON"	"OFF"	Executes the step advance type program and advances according to the programmed conditions. After the execution of the STEP END instruction, the program automatically returns to step 01.
"—"	"—"	"—"	"OFF"	"OFF"	Executes the manual program.
"OFF"	"ON"	"OFF"	"ON"	"OFF"	Executes the step advance type program and advances by the forced advance (Advance input) "1."
"—"	"—"	"—"	"—"	"ON"	Executes nothing and waits at step 01.

NOTE: "—" Dash indicates that the condition of this relay number is not considered for the function to operate.

4.3.6 Relationship between address number and step number

In the ladder diagram programming method, a location where a program is written is expressed as an "address," whereas in the step advance type programming method, the same is expressed as a "step."



- **Program capacity**

  When programs are to be written using both the ladder diagram and step advance type methods, add the word lengths of all the instructions to be used by referring to the word length of each instruction indicated in the list of instructions, so that the programs to be written do not exceed the max. memory capacity. Note that 7 addresses correspond to one step.

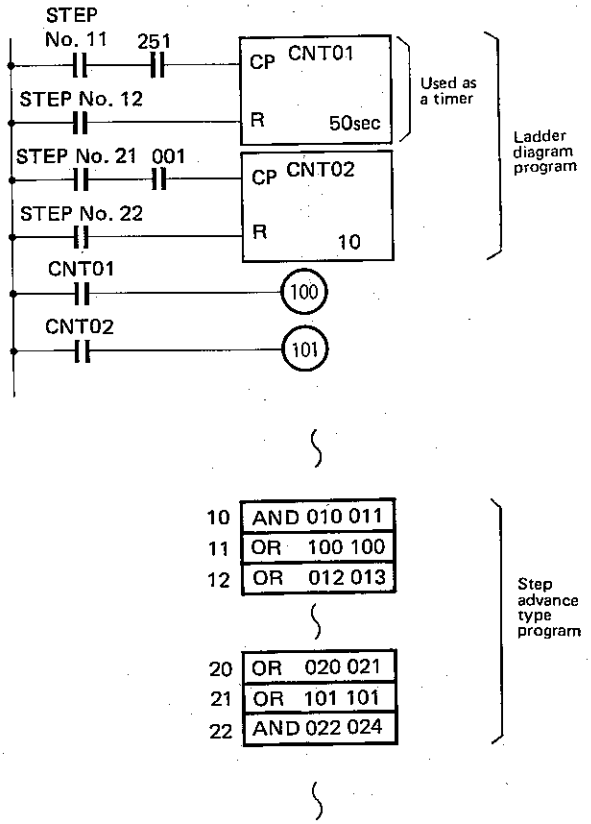
Address	Step	OP	Data	Word length
0000		LD	000	1W
0001		OR	066	1W
0002		AND	001	1W
0003		AND	002	1W
0004		OUT	066	1W
0005		LD	100	1W
0006		AND-NOT-TIM	01	1W
0007		OR	003	1W
0008		OUT	100	1W
0009		LD	100	1W
0010		TIM	01	2W
0011			050	
0012		LD	100	1W
0013		AND-NOT-TIM	01	1W
0014		OUT	067	1W
0015		LD	004	1W
0016		LD	005	1W
0017		LD	006	1W
0018		LD	007	1W
0019		LD	008	1W
0020		STEP-CON	0	1W
0021 ~ 0027	01	AND	066 011	7W
0028 ~ 0034	02	OR	012 012	7W
0035 ~ 0041	03	TIM	100 000	7W
0042 ~ 0048	04	AND	011 100	7W
0049 ~ 0055	05	TIM	200 000	7W
0056 ~ 0062	06	STEP-END		7W
0063		LD	009	1W
0064		AND-NOT	011	1W
0065		OUT	050	1W
0066		LD	010	1W
0067		AND-NOT	012	1W
0068		OUT	051	1W
0069		LD	013	1W
0070		AND-NOT	014	1W
0071		OUT	052	1W
0072		MANU-END		1W
0073		END		1W
0074				
⋮		⋮		
2047				

NOTE: Addresses in ▭ will not be displayed, but only their corresponding steps will be displayed.

4.3.7 Applied program

■ **To retain the present value of a timer/counter in memory when a power failure occurs.**

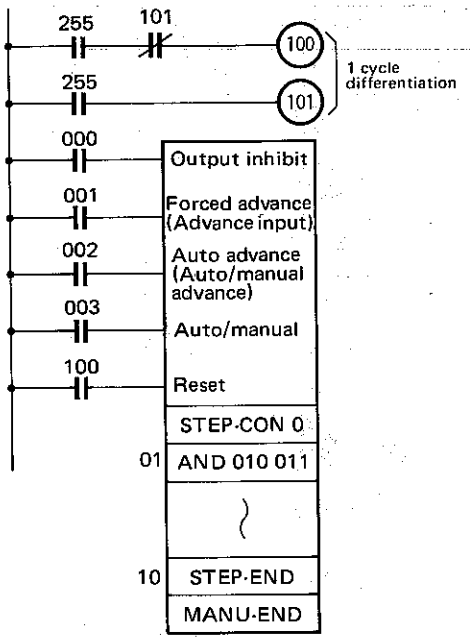
When a power failure occurs, all the data except the step number are cleared from memory. Therefore, if the present value of a timer or counter is to be retained in memory, use a ladder diagram instruction CNT to process the internal auxiliary relay and then process the result with an OR (or AND) instruction.



Address	Step	OP		Data
0200		LD· STEP NO.		11
0201		AND		251*
0202		LD· STEP NO.		12
0203		CNT		01
0204				050
0205		LD·STEP NO.		21
0206		AND		001
0207		LD·STEP NO.		22
0208		CNT		02
0209				010
0210		LD·CNT		01
0211		OUT		100
0212		LD·CNT		02
0213		OUT		101
⟆		⟆		
0350 ~ 0356	10	AND	010	011
0357 ~ 0363	11	OR	100	100
0364 ~ 0370	12	OR	012	013
⟆		⟆		
0420 ~ 0426	20	OR	020	021
0427 ~ 0433	21	OR	101	101
0434 ~ 0440	22	AND	022	024
⟆	⟆	⟆		

NOTE: * Special auxiliary relay No. 251 generates 1sec clock.

■ **To start from step 01 upon recovery from power failure**



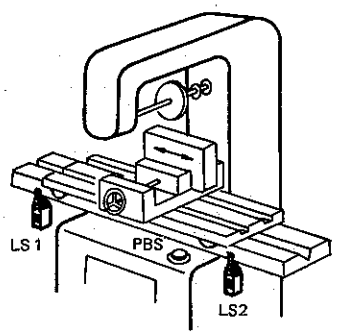
Address	Step	OP		Data
0200		LD		255
0201		AND·NOT		101
0202		OUT		100
0203		LD		255
0204		OUT		101
0205		LD		000
0206		LD		001
0207		LD		002
0208		LD		003
0209		LD		100
0210		STEP·CON		0
0211 ~ 0217	01	AND	010	011
⟆	⟆	⟆		
0274 ~ 0280	10	STEP·END		
0281		MANU·END		

NOTES:
1. Internal auxiliary relay 255 is normally ON.
2. Using internal auxiliary relay 255, prepare 1 cycle differentiation (at the time of the power failure) and apply it to the result of STEP CON.

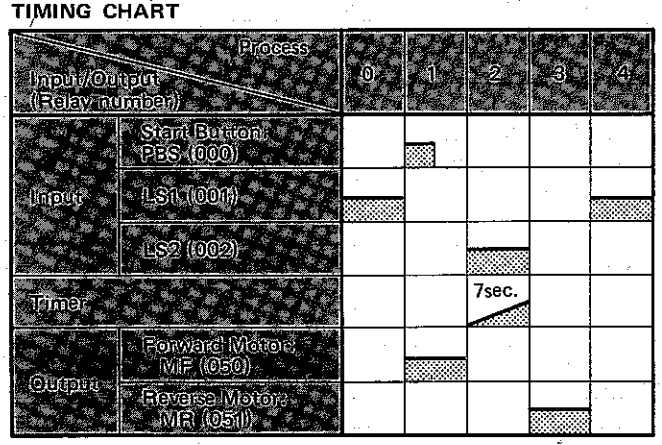
4.3.8 Programming examples

- **Operation of machine tool**

1. When start button (PBS) is depressed in the condition of LS1: ON, forward motor (MF) turns ON, that is, the work table starts moving to the right side.
2. When the moving table turns ON the LS2 at the right, the forward motor stops. At the same time, the timer starts to count.
3. Reverse motor (MR) turns ON after the timer counts up 7 seconds, that is, the table starts moving to the left side.
4. When the moving table turns ON the LS1 at the left, the reverse motor stops.



TIMING CHART

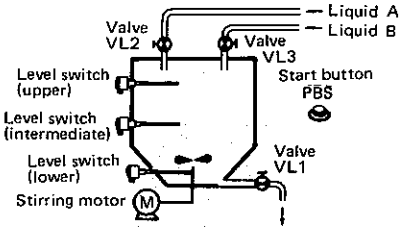


CODING

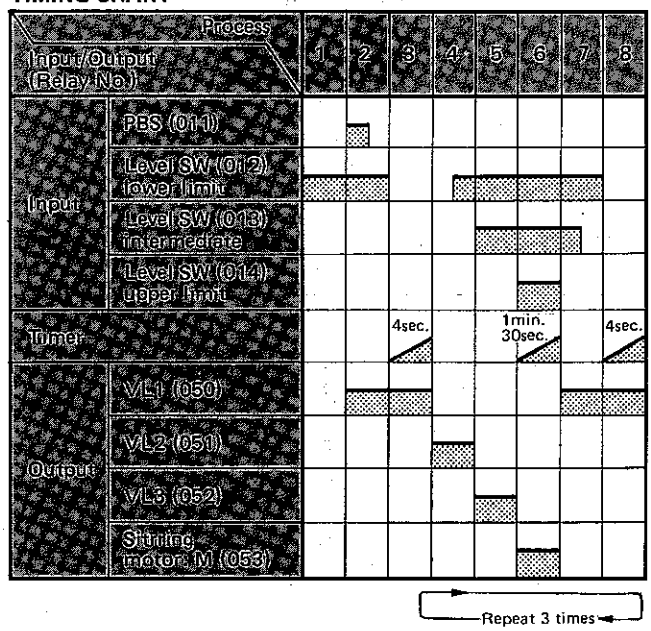
Address	STEP No.	OP	Data		Output				
			DATA-1	DATA-2	050	051	052	053	054
0020		STEP CON		0					
0021 ~ 0027	01	AND	000	001					
0028 ~ 0034	02	OR	002	002	ON				
0035 ~ 0041	03	TIM	070	000					
0042 ~ 0048	04	OR	001	001		ON			
0049 ~ 0055	05	STEP END							
0056		MANU END							

- **Operation of liquid level control**

1. When start button (PBS) is depressed, valve (VL1) is caused to open so that mixed liquid A, B is discharged down to the lower-limit level. After the above process, valve (VL1) is still open for 2 seconds to discharge the remaining liquid.
2. Valve (VL2) is caused to open to start the infusion of liquid A.
3. When liquid A is infused up to the intermediate level, valve (VL3) is caused to open to start the infusion of liquid B.
4. When mixed liquid A, B is infused up to the upper-limit level, the stirring motor is caused to turn ON for 1 min. 30 sec.
5. The above process (discharge → infusion of liquid A → infusion of liquid B → stirring) is repeated 3 times.
6. Discharge.



TIMING CHART

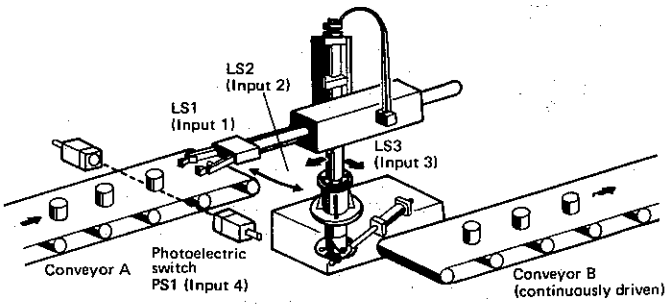


CODING

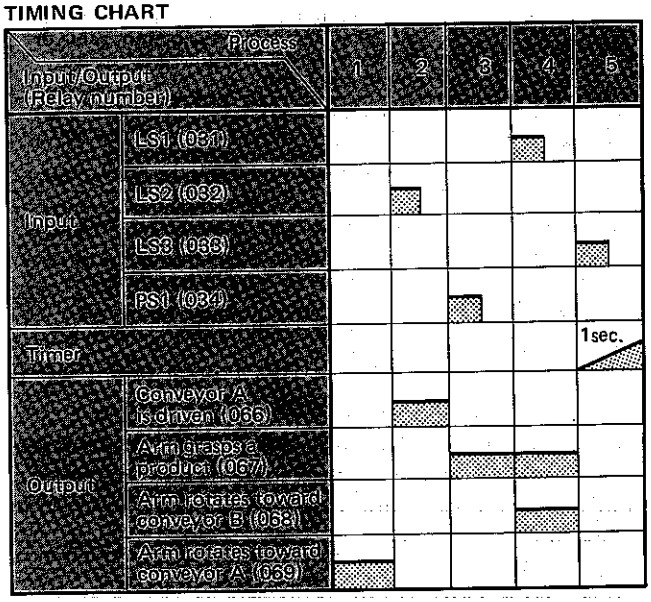
Address	STEP No.	OP	Data		Output				
			DATA-1	DATA-2	050	051	052	053	054
0200 ~ 0201		LD·STEP NO.		001					
0202 ~ 0203		LD·STEP NO.		008					
0204		CNT		10					
0205				003					
0206		LD·CNT		10					
0207		OUT		100					
0208		LD		000					
0209		LD		001					
0210		LD		002					
0211		LD		003					
0212		LD		004					
0213		STEP·CON		0					
0214 ~ 0220	01	OR	011	011					
0221 ~ 0227	02	OR	012	012	ON				
0228 ~ 0234	03	TIM	040	000	ON				
0235 ~ 0241	04	AND	012	013		ON			
0242 ~ 0248	05	OR	014	014			ON		
0249 ~ 0255	06	TIM	090	001				ON	
0256 ~ 0262	07	CJP	010	100					
0263 ~ 0269	08	OR	012	012	ON				
0270 ~ 0276	09	TIM	040	000	ON				
0277 ~ 0283	10	STEP·END							
0284		MANU·END							

- **Operation of robot**

The movements of an industrial robot arm to transfer products from conveyor A to conveyor B, such as forward and backward, up and down, grasp, release, etc., are controlled by the step controller. Though the operations of the robot are sophisticated, the grasping, releasing and rotating movements only of the arm are simply taken up for the purpose of programming.



TIMING CHART



CODING

Address	STEP No.	OP	Data		Output				
			DATA-1	DATA-2	066	067	068	069	070
0050		STEP·CON		1					
0051 ~ 0057	01	OR	032	032				ON	
0058 ~ 0064	02	OR	034	034	ON				
0065 ~ 0071	03	OR	031	031		ON			
0072 ~ 0078	04	OR	033	033		ON	ON		
0079 ~ 0085	05	TIM	010	000					
0086 ~ 0092	06	STEP·END							
0093		MANU·END							

4.4 Operating procedure

4.4.1 Basic functions

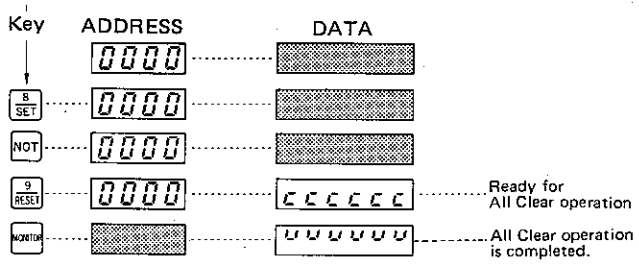
Items of operation	Description
All program clear	Since the CPU retains previously stored data in memory (by battery back-up), all the memory contents must be cleared to write a new program into the memory.
Address setting	Address setting is required to designate an address in such operations as program read, program write, etc.
Program write	This operation is to store a program in the specified memory address.
Program read	This operation is to confirm whether or not data has been programmed properly in the specified memory address.
Program check	This operation is to confirm whether or not the program data written into the CPU memory through the program console are in agreement with the predetermined rules (syntax).
RUN	This operation is to place the SYSMAC-P5R in the RUN (Program Execution) state.
Monitor	This operation is to display the operating state of each relay, or the present value of each timer or counter during the execution of a program.
Step search	When a circuit change is to be made in a program simulation or test run, this operation allows an address where a step has been written in a program to be searched.
Instruction change	This operation is to change instruction(s) in a program due to a circuit modification.
Instruction addition	This operation is to add instruction(s) to a program due to a circuit modification.
Instruction deletion	This operation is to delete the instruction(s) from a program due to a circuit modification.

4.4.2 All program clear operation

Since the CPU retains previously stored data in memory (by battery back-up), all the memory contents must be cleared to write a new program into the memory.

- **Operating procedure**

- **Display**



NOTES:

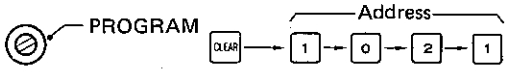
1. By the All Clear operation, all the programs (I/O relays, internal auxiliary relays, latching relays, timers and counters) stored in the memory are cleared.
2. Before the key operation, change the mode selector switch position from "PROM WRITER" to "PROGRAM."
3. In the All Clear operation, a beep sound is generated at the depression of each key.
4. Upon depression of the MONITOR key, the ADDRESS display is extinguished. However, subsequent depression of the CLEAR key causes the ADDRESS display to indicate "0000."

CAUTION:
After the PROGRAM mode selection, depression of CLEAR key or any key other than the four keys shown above will not allow All Clear operation to be executed. In this case, repeat the operation starting from the mode selection.

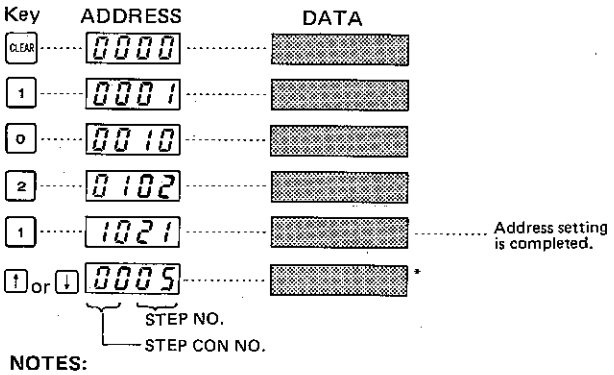
4.4.3 Address setting operation

Address setting is required to designate an address in such operations as program read, program write, etc.

- **Operating procedure**

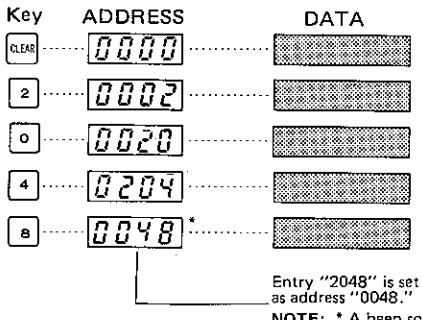


- **Display**



NOTES:

1. Each address is set in 4 digits using numeric data. To set address "0000," no numeric entry is required. To set address "0003," depress only numeric key 3 and to set address "0023," depress only numeric keys 2 and 3. Preceding zero(s) may be omitted from key entry.
2. * The step No. and data entered will not be displayed by the address setting operation alone. To display these, ↑ or ↓ keys must be depressed. Since each step corresponds to 7 addresses, depress one of the 7 addresses and the corresponding step No. and data will be displayed.
3. In address setting, when numeric data entered as an address exceeds the max. memory capacity, the first two digits of the 4-digit address are automatically processed as "0." Since the CPU does not recognize this as an error, the only way to identify this error is through confirmation by the operator. For example, with the SCY-P5R30E, if address 2048 is entered, it will be set as follows.

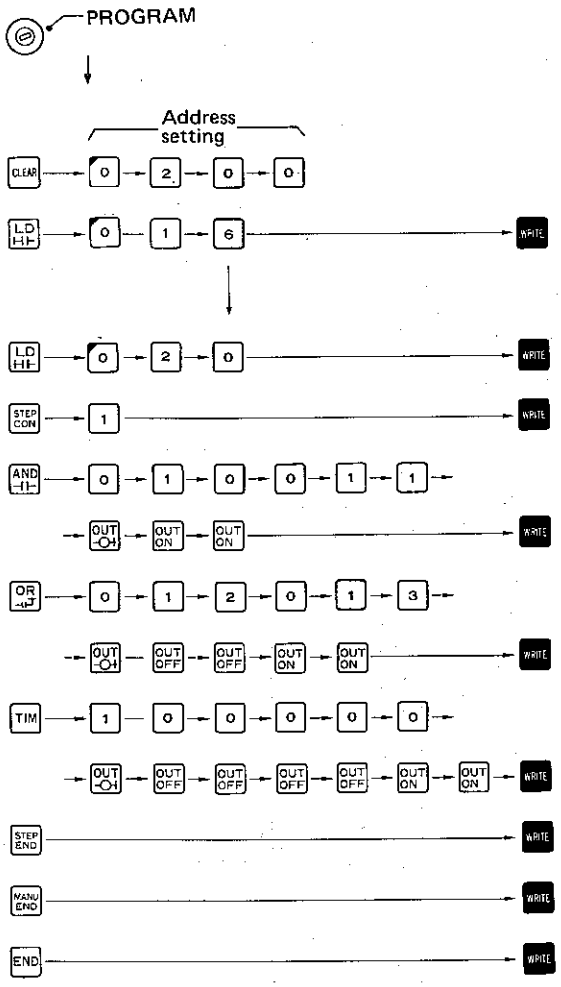


NOTE: * A beep sound will be heard then.

4.4.4 Program write operation

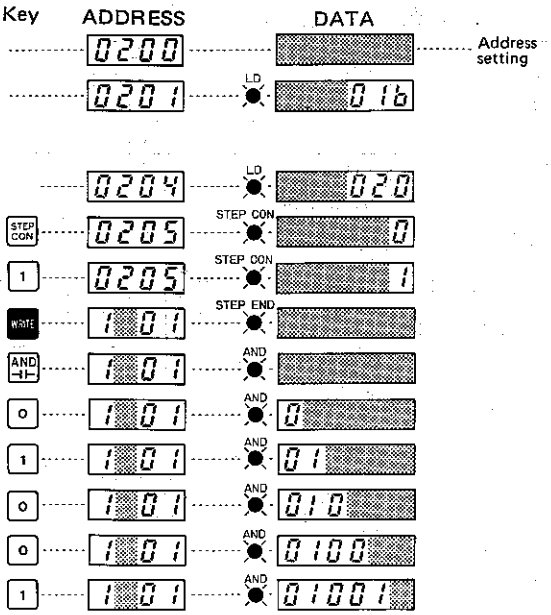
This operation is to store a program in the specified memory address.

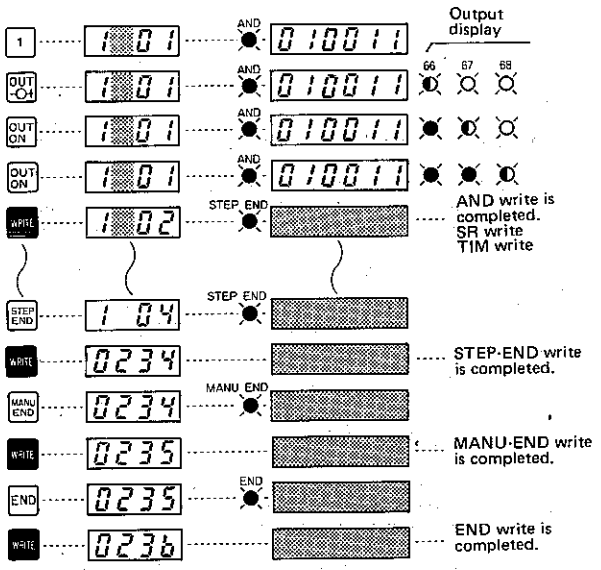
- **Operating procedure**



NOTE: The zero key marked [0] may or may not be depressed.

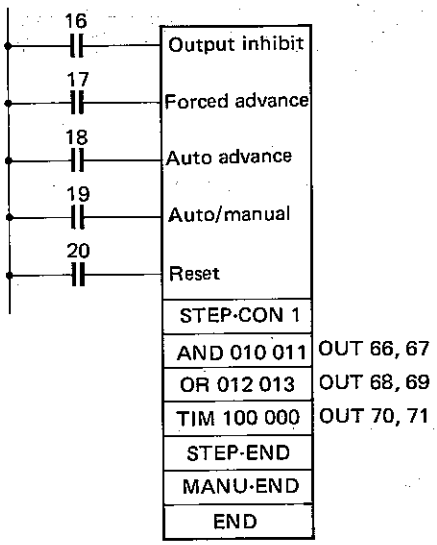
- **Display**





NOTE: denotes that the indicator lights.
denotes that the indicator goes out.
denotes that the indicator flashes ON and OFF.

- **Circuit for exercise and programming example**



Address	Step	OP	Data		Output
0200		LD		016	
0201		LD		017	
0202		LD		018	
0203		LD		019	
0204		LD		020	
0205		STEP-CON		1	
0206~0212*	01	AND	010	011	66,67
0213~0219	02	OR	012	013	68,69
0220~0226	03	TIM	100	000**	70,71
0227~0233	04	STEP-END			
0234		MANU-END			
0235		END			

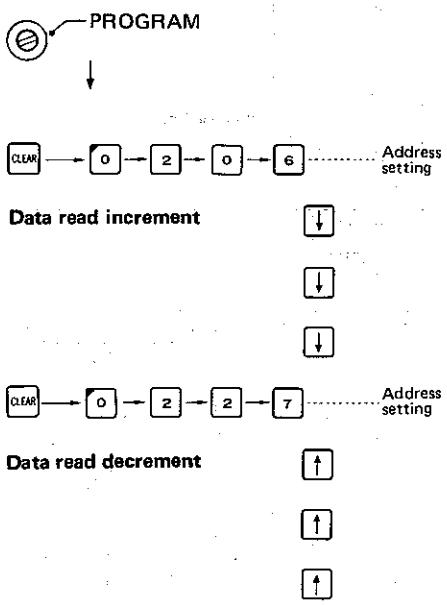
NOTES:
1. Entry of a STEP CON instruction causes an address to change to a step (e.g., 0205 → 01), and the ADDRESS display continues to indicate the step until a STEP END instruction is entered. Upon entry of the STEP END instruction, the ADDRESS display changes from a step to an address (e.g., 04 → 0234).
2. * 7 addresses correspond to one step.
3. ** The data for CJP, AND, OR, TIM and CNT instructions in a step advance type program must always be entered in 3 digits.
4. To write a program, observe the following key operation sequence.
   [OP key] + [Numeric key] + [Numeric key] + [Output setting]
5. Depression of the WRITE key causes the data appearing on the OP, DATA and OUTPUT displays to be stored in memory.
6. Depression of the WRITE key causes steps to increment by 1 and the data of the step number incremented to be displayed.
7. In other than PROGRAM mode, if a numeric error exists, each depression of the WRITE key causes a beep sound to be generated to alert the operator.
   Check for the proper operating procedure, and retry the correct key input operation.

Correction procedures when an error occurs in program write
1. If a programming error is noticed before depressing the WRITE key, depress the CLEAR DISPLAY key followed by the key operation [OP key] + [Numeric key] + [Numeric key] + [Output setting] and then depress the WRITE key.
2. If an error is discovered after the depression of the WRITE key, try the step search operation or return the program to the step where the error exists by using the key and then depress the following keys: [CLEAR DISPLAY] + [OP] + [Numeric] + [Numeric] + [Output setting] + [WRITE]

4.4.5 Program read operation

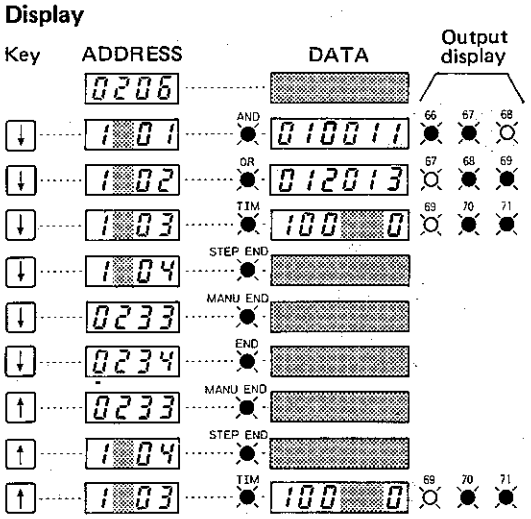
This operation is to confirm whether or not the data has been programmed properly in the specified memory address.

- **Operating procedure**

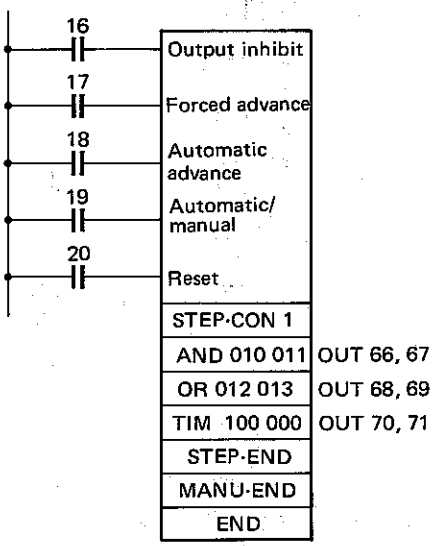


NOTE: The zero key marked [0] may or may not be depressed.

- **Display**



- **Circuit for exercise and programming example**



Address	Step	OP	Data		Output
0200		LD		016	
0201		LD		017	
0202		LD		018	
0203		LD		019	
0204		LD		020	
0205		STEP-CON		1	
0206~0212	01	AND	010	011	66, 67
0213~0219	02	OR	012	013	68, 69
0220~0226	03	TIM	100	000	70, 71
0227~0233	04	STEP-END			
0234		MANU-END			
0235		END			

NOTES:
1. When an address in a step advance type program is set and then read by the [↑] or [↓] key, the address entered will automatically change to its corresponding step and will be displayed. (For example, addresses 0213 through 0219 will be displayed as step 02.)
2. Direct step No. setting is not possible in all the operations except step search operation.

4.4.6 Program check operation

This operation is to confirm whether or not the program data written into the CPU memory through the program console are in agreement with the predetermined rules (syntax).

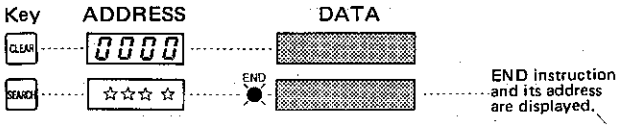
Items subject to program check are as follows.

- Coil duplication error
- STEP-STEP-END error
- Format error
- END instruction missing error

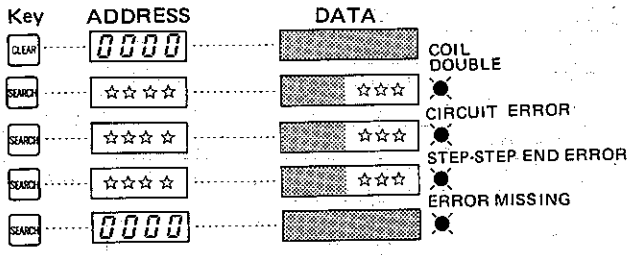
- **Operating procedure**

- **Display**

When a program error does not exist.



When a program error exists.



- **Error conditions**

1. Coil duplication error
   When a step advance type program is used in conjunction with a ladder diagram program, the "COIL DOUBLE" indicator illuminates if the output relay No. used in the ladder diagram is used again in the step advance program. [However, this relationship does not exist in a step advance program and its manual (ladder diagram) program.]
2. STEP-STEP END error
   (1) Be sure to use STEP CON, STEP END, and MANU END instructions in this combination. If they are used in other than this combination, the "STEP-STEP END ERROR" indicator illuminates.
   (2) If the group number 0, 1 or 2 of a STEP CON instruction is used in duplication, the "STEP-STEP END ERROR" indicator also illuminates.
3. Format error
   The "FORMAT ERROR" indicator illuminates if any instruction not conforming with the specified format is found during a program check.
4. END instruction missing error
   The "END MISS" indicator illuminates if no END instruction exists at the end of a program.

NOTES:

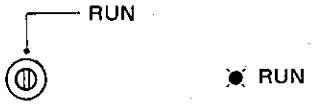
1. If any programming error is discovered, correct the erroneous program in accordance with the program write procedure.
2. Even if a coil duplication error occurs, the CPU can still perform the RUN or MONITOR operation. However, be sure to correct this error to execute the proper program.
3. Should any of the following errors occur, the CPU can perform neither the RUN nor MONITOR operation.
   - STEP-STEP END error
   - Format error
   - END instruction missing error

   Be sure to correct the erroneous program.

4.4.7 RUN operation

This operation is to place the SYSMAC-P5R in the RUN (Program Execution)

- **Operating procedure**



NOTES:

1. In the absence of an END instruction in a program, the RUN indicator will not illuminate even if the operation mode of the CPU is changed to "RUN." (All keys become inoperative.) At the same time, the "END MISS" indicator illuminates and the alarm buzzer sounds. In this case, change the operation mode to "PROGRAM" and enter an END instruction to correct the program.
2. After the CPU starts operating, if an error occurs as a result of a parity check or watchdog timer check, the RUN indicator goes out and the following conditions take place.
   (1) If a parity error occurs, the MEMORY FAILURE indicator illuminates and the memory/CPU fault output (control I/O relay) is ON and the ON/OFF states of all external outputs are held as is.
   (2) If a watchdog timer error occurs, the CPU FAILURE indicator illuminates and the memory/CPU fault output (control I/O relay) is ON and all external outputs are turned off.

   Refer to 7.4, Troubleshooting for details.
3. In other than the RUN and MONITOR modes, all external outputs are turned off. When the mode selector switch position is changed from other mode to "RUN," the SYSMAC-P5R is placed in the same state when power is applied.

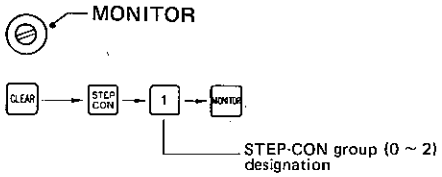
4.4.8 Monitor operation

This operation is to display the operating state of each relay, or the present value of each timer or counter during the execution of a program.

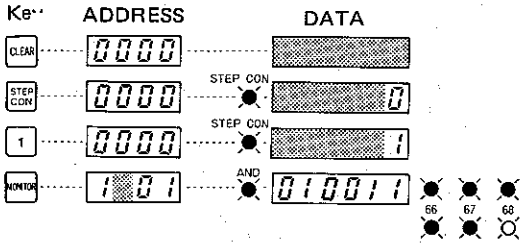
■ MONITORING OF ONLY THE SPECIFIED STEP CONTROLLER GROUP

In this case, the step being executed, the operating state of each relay, and the present value of each timer or counter are displayed.

- **Operating procedure**



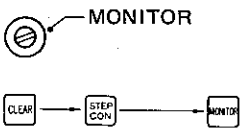
- **Display**



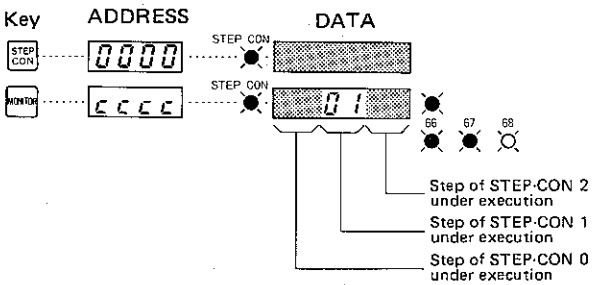
■ PARALLEL MONITORING OF 3 STEP CONTROLLER GROUPS

In this case, only the step being executed of each step controller group and the present value of each timer or counter are displayed.

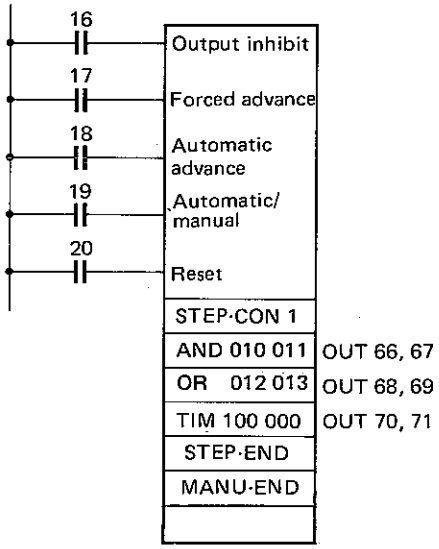
- **Operating procedure**



- **Display**



- **Circuit for exercise and programming example**



Address	Step	OP	Data		Output
0200		LD		016	
0201		LD		017	
0202		LD		018	
0203		LD		019	
0204		LD		020	
0205		STEP-CON		1	
0206~0212	01	AND	010	011	66, 67
0213~0219	02	OR	012	013	68, 69
0220~0226	03	TIM	100	000	70, 71
0227~0233	04	STEP-END			
0234		MANU-END			
0235		END			

NOTES:

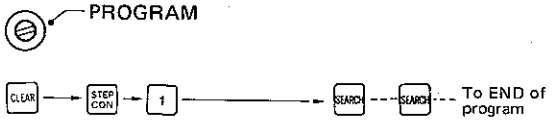
1. In the step advance type programming, only the step and instruction being executed and the operating condition of each step controller group can be monitored. For example, in the example shown on the left, step 01 of STEP CON 1 is under execution. The instruction is AND 010, 011. The operating condition of the group is Automatic advance.
2. By the key operation CLEAR → STEP CON → 1 → MONITOR, only the STEP CON 1 group is monitored to check the step and instruction being executed and the operating condition of the group.
3. By the key operation CLEAR → STEP CON → MONITOR, only the step being executed by each step controller group can be checked.

4.4.9 Step search operation

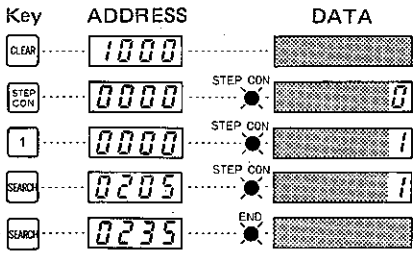
When a circuit change is to be made in a program simulation or test run, this operation allows an address where a step has been written in a program to be searched.

■ SEARCH OF THE STEP CON INSTRUCTION(S) OF THE SPECIFIED STEP CONTROLLER GROUP

- **Operating procedure**

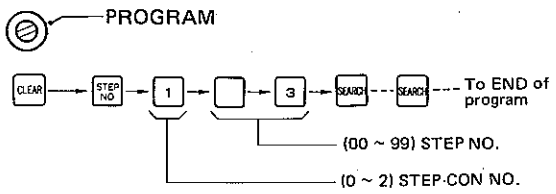


- **Display**

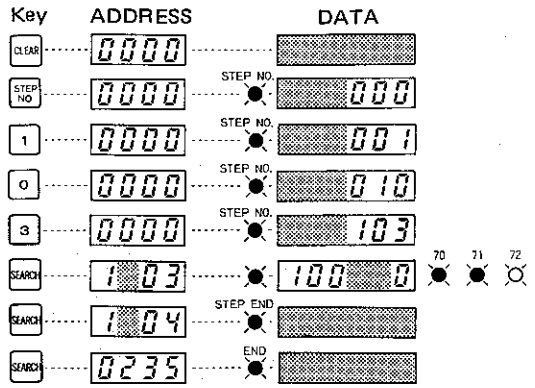


■ SEARCH OF ANY STEP OF THE SPECIFIED STEP CONTROLLER GROUP

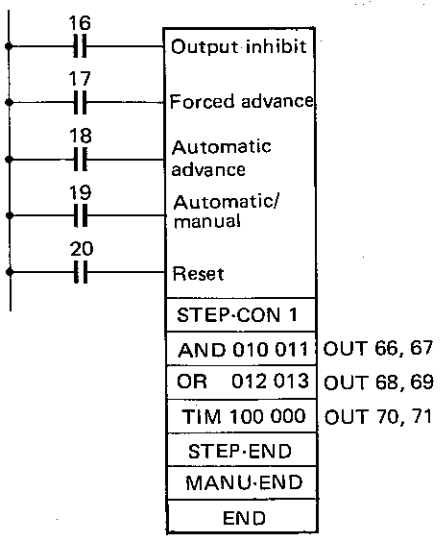
- **Operating procedure**



- **Display**



- **Circuit for exercise and programming example**



Address	Step	OP	Data		Output
0200		LD		016	
0201		LD		017	
0202		LD		018	
0203		LD		019	
0204		LD		020	
0205		STEP-CON		1	
0206~0212	01	AND	010	011	66, 67
0213~0219	02	OR	012	013	68, 69
0220~0226	03	TIM	100	000	70, 71
0227~0233	04	STEP-END			
0234		MANU-END			
0235		END			

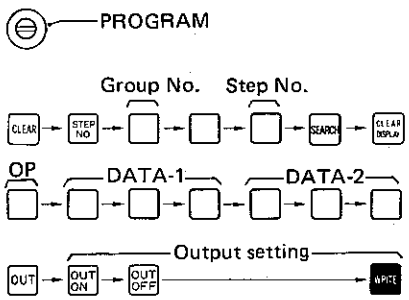
NOTES:
1. Except for steps 01 through 04 in the above program, search of an instruction is possible as follows.
   CLEAR → OP → WRITE → SEARCH
2. In the above program, instructions at steps 01 through 04 cannot be searched. Only the step search is possible as shown on the left.

4.4.10 Instruction change operation

This operation is to change instruction(s) in a program due to a circuit modification.

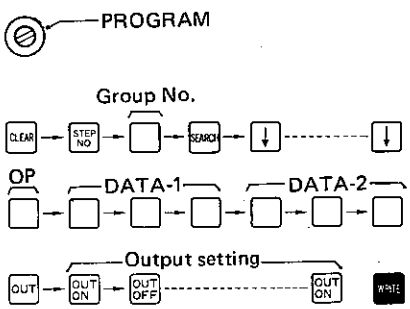
■ TO START FROM THE STEP TO BE CHANGED

- **Operating procedure**



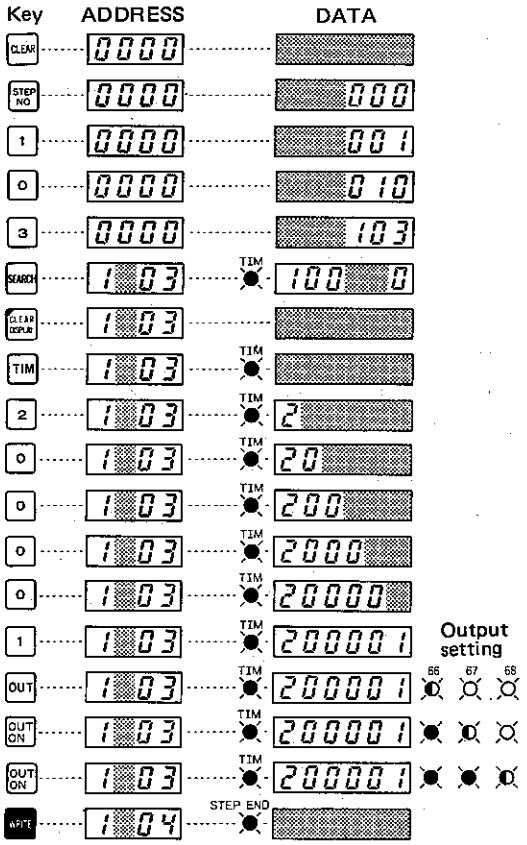
■ TO START FROM THE BEGINNING (STEP CON INSTRUCTION) OF A STEP ADVANCE PROGRAM

- **Operating procedure**



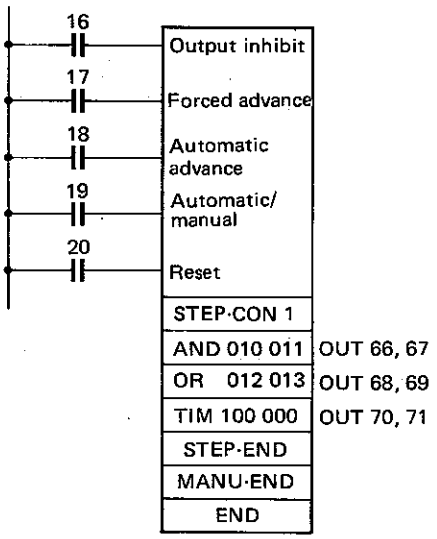
- **Display**

(Example) Changes to the timer set value and output and output of the step 03 of STEP CON group 1



NOTE: The key marked [CLEAR DISPLAY] may or may not be depressed.

- **Circuit for exercise and programming example**



Address	Step	OP	Data		Output
0200		LD		016	
0201		LD		017	
0202		LD		018	
0203		LD		019	
0204		LD		020	
0205		STEP·CON		1	
0206~0212	01	AND	010	011	66, 67
0213~0219	02	OR	012	013	68, 69
0220~0226	03	TIM	100	000	70, 71
0227~0233	04	STEP·END			
0234		MANU·END			
0235		END			

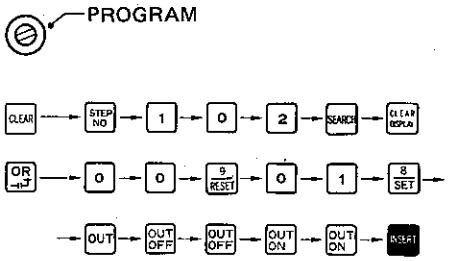
Address	Step	OP	Data		Output
0200		LD		016	
0201		LD		017	
0202		LD		018	
0203		LD		019	
0204		LD		020	
0205		STEP·CON		1	
0206~0212	01	AND	010	011	66, 67
0213~0219	02	OR	012	013	68, 69
0200~0226	03	TIM	200	001	66, 67
0227~0233	04	STEP·END			
0234		MANU·END			
0235		END			

NOTES:
1. To change an instruction, instruction and output settings must all be performed from the beginning.
2. After the instruction change, be sure to perform the program check operation by depressing the CLEAR key and SEARCH key to confirm that no error exists in the program.
3. If a program is desired to be added before the STEP END instruction, first search a step into which the STEP END instruction has been written and then write the program to be added into the searched location. In this case, be careful not to cause a program over condition, as STEP END, MANU END and END instructions move downward by 7 words respectively at each addition of a one-step instruction.

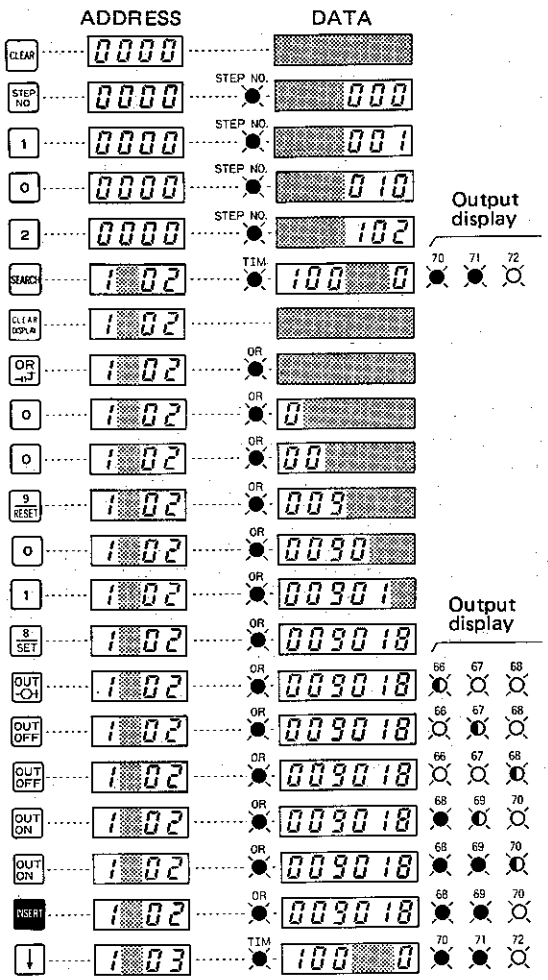
4.4.11 Instruction addition operation

This operation is employed when the instruction is to be added due to a circuit modification.

- **Operating procedure**



- **Display**

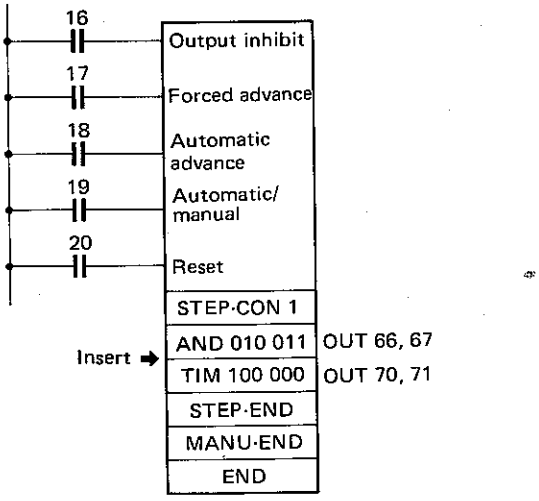


Address	Step	OP	Data		Output
0200		LD		016	
0201		LD		017	
0202		LD		018	
0203		LD		019	
0204		LD		020	
0205		STEP·CON		1	
0206~0212	01	AND	010	011	66, 67
0213~0219	02	TIM	100	000	70, 71
0220~0226	03	STEP·END			
0227		MANU·END			
0228		END			

Address	Step	OP	Data		Output
0200		LD		016	
0201		LD		017	
0202		LD		018	
0203		LD		019	
0204		LD		020	
0205		STEP·CON			
0206~0212	01	AND	010	011	66, 67
0213~0219	02	OR	009	018	68, 69
0220~0226	03	TIM	100	000	70, 71
0227~0233	04	STEP·END			
0234		MANU·END			
0235		END			

NOTES:
1. STEP CON or STEP END instruction cannot be inserted independently, as they must always be used in pairs.
2. When one step of step advance instruction is inserted, addresses subsequent to the inserted step will be increased by 7.

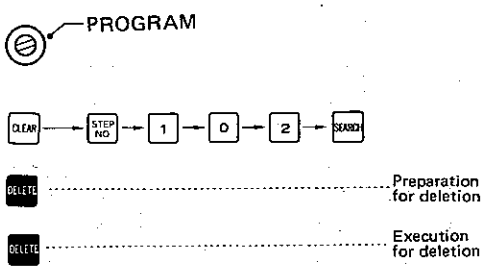
- **Circuit for exercise and programming example**



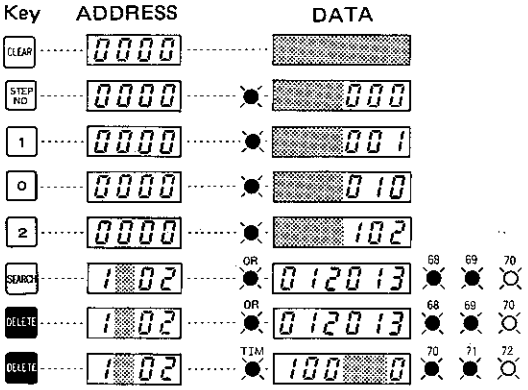
4.4.12 Instruction deletion operation

This operation is to delete instruction(s) from a program due to a circuit modification.

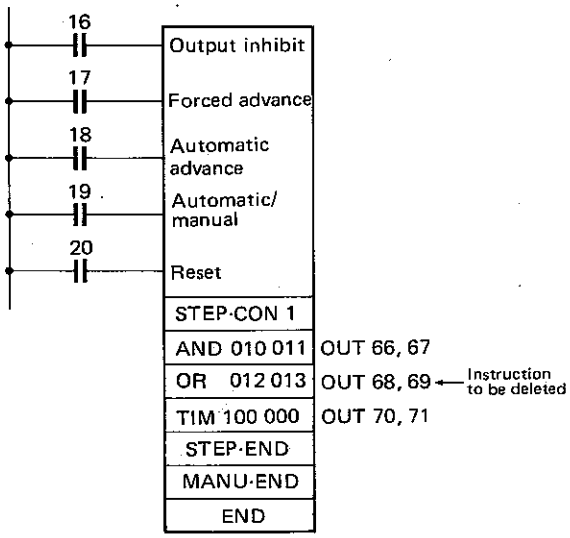
- **Operating procedure**



- **Display**



- **Circuit for exercise and programming example**



Address	Step	OP	Data		Output
0200		LD		016	
0201		LD		017	
0202		LD		018	
0203		LD		019	
0204		LD		020	
0205		STEP·CON		1	
0206~0212	01	AND	010	011	66, 67
0213~0219	02	OR	012	013	68, 69
0220~0226	03	TIM	100	000	70, 71
0227~0233	04	STEP·END			
0234		MANU·END			
0235		END			

⬇

Address	Step	OP	Data		Output
0200		LD		016	
0201		LD		017	
0202		LD		018	
0203		LD		019	
0204		LD		020	
0205		STEP·CON		1	
0206~0212	01	AND	010	011	66, 67
0213~0219	02	TIM	100	000	70, 71
0220~0226	03	STEP·END			
0227		MANU·END			
0228		END			

NOTES:

1. Search an OUT instruction, depress the ↑ key to advance the program up to the address where the instruction to be deleted is located, and depress the DELETE key twice in succession. All the address numbers after the deleted instruction will automatically be decremented by 1.
   The reason for depressing the DELETE key twice is to prevent an instruction from being deleted accidentally due to an erroneous key operation. The first depression of the key causes a beep sound to be generated to signal the preparation for an instruction deletion. The second and each subsequent depression of the key cause instructions to be deleted one by one.
2. When a STEP CON instruction is deleted, all instructions up to the MANU END instruction of that group will be deleted.
3. A STEP END instruction cannot be deleted independently.
4. When one step of step advance instrudtion is deleted, addresses subsequent to the deleted step will be decreased by 7.

5. EPROM Chip and Cassette Tape Handling

5.1 Basic Functions

Items of operation	Description
EPROM write	This operation is to transfer the contents of the RAM to the specified EPROM area.
EPROM read	This operation is to transfer the contents of the specified EPROM area to the RAM.
EPROM verify	This operation is to verify the contents of the specified EPROM area against the contents of the RAM.
Tape write	This operation is to record the contents of the RAM (program memory) on a cassette tape.
Tape read	This operation is to transfer the program data recorded on the cassette tape into the RAM.
Tape verify	This operation is to verify the contents of the RAM against the programmed data recorded on a cassette tape.

5.2 EPROM Handling

Since Type SCY-P5R executes programs by reading the contents of the RAM, Type SCY-P5R permits data read, write and verify operations between the RAM and the EPROM when various programs are in use, or for program storage.

■ AVAILABLE TYPE OF EPROM

Type ROM-2732 (equivalent to 2732)

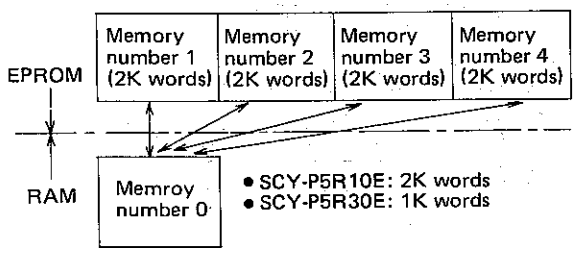
■ MEMORY CAPACITY

4 kinds of user programs (1k or 2k RAM addresses x 4) can be stored per EPROM chip.

■ ADDRESS SETTING

The EPROM address area is divided into 4, which are referred to as memory numbers 1, 2, 3 and 4, respectively.

EPROM Memory No. Configuration*

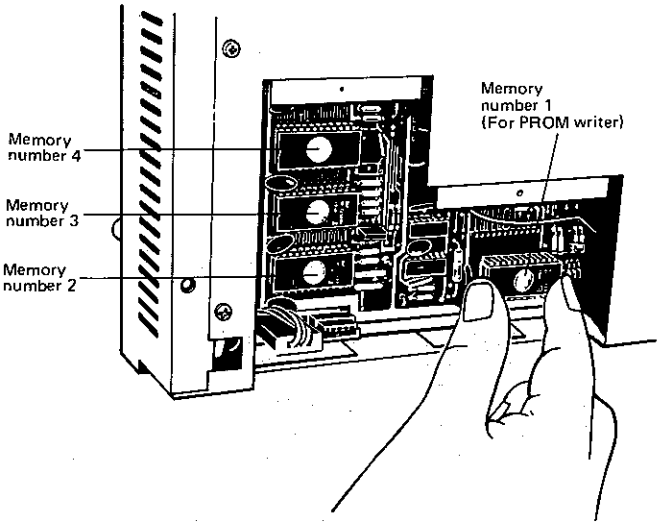


RAM Memory No. Configuration

NOTES:
1. EPROM write: Data transfer from memory No. 0 to memory No. 1 only.
2. EPROM read: Data transfer from any of memory Nos. 1 ~ 4 to memory No. 0.
3. EPROM verify: Data verification between memory No. 0 and any of memory Nos. 1 ~ 4.
4. Memory No. must be specified using keys on the front panel of the CPU.
5. * With the SCY-P5R30E, an EPROM chip with a capacity of 2K words (ROM-2732) is provided for each of memory Nos. 1 thru 4. However, only 1K words of the 2K words are permitted for practical use.

■ MOUNTING EPROM CHIP

Be sure to insert the EPROM chip onto the EPROM socket with its dip facing upwards.

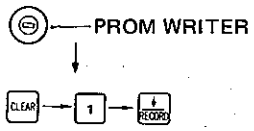


NOTES:
1. Completely erase the EPROM and then write data into the EPROM. The contents of the EPROM are erased by irradiating ultraviolet rays on the EPROM surface through the erase window. The EPROM cannot be erased completely if the irradiation of ultraviolet rays is insufficient. Therefore, be sure to observe the specified erase time. Whether or not the EPROM has been erased completely can be confirmed by the EPROM Verify operation. (Refer to paragraph 5.6, Errors in PROM WRITER Mode.)
2. Erase time
   Completely erase the EPROM according to the specifications of the eraser to be used.
3. Frequency of re-programming
   Limit the frequency of re-programming the EPROM to 7 times. If the EPROM is re-programmed more than 7 times, the EPROM may malfunction.
4. Program protection
   To sustain the reliability of the EPROM, place the EPROM in a protective case or wrap it in aluminum foil if it is not to be used for an extended period.
5. Handling EPROM
   The EPROM is susceptible to static electricity being carried in the human body. When handling the EPROM avoid touching its pins as much as possible.
6. Removal of EPROM
   Only the EPROM chip inserted into memory No. 1 can be removed or reinserted while power is being applied to the SYSMAC-P5R. However, never remove the EPROM chip during the EPROM write, read, or verify operation.
7. When removing the EPROM chip from the EPROM socket, be sure to turn off the power being supplied to the CPU.
8. After the program debugging, be sure to attach a light-shielding seal to the erase window in order to maintain the reliability of the EPROM chip.

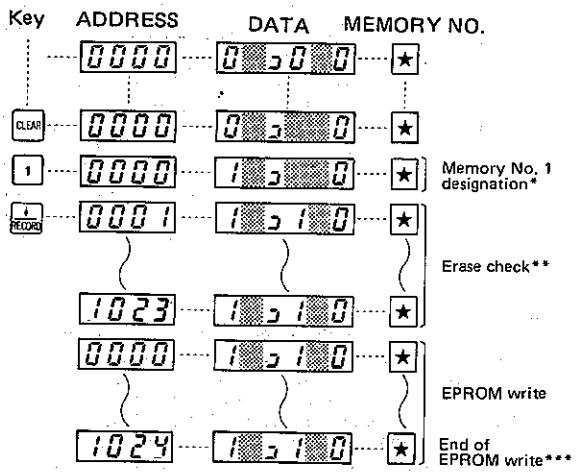
5.3 EPROM Write Operation

This operation is to transfer the contents of the RAM to the No. 1 EPROM memory.

- **Operating procedure**



- **Display**

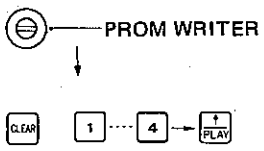


NOTES:
1. * Be sure to set the memory number to "1."
2. ** Upon depression of RECORD key, EPROM erase check is performed, and then the EPROM write operation will start.
3. During the EPROM write operation, if the power is turned off, or the EPROM chip is removed, the EPROM write will be interrupted. In such a case, retry the EPROM write operation from the beginning after erasing the EPROM chip, or use other EPROM area.
4. During the EPROM write operation, no PROGRAM key input will be accepted.
5. *** When the EPROM write operation is completed or when any error occurs during the EPROM write operation, the buzzer issues intermittent beep sounds to alert the operator.
6. After the EPROM write operation, be sure to perform the EPROM Verify operation to check if the data have been written properly into the EPROM.
7. Approx. 4 minutes are required to complete one EPROM write operation.

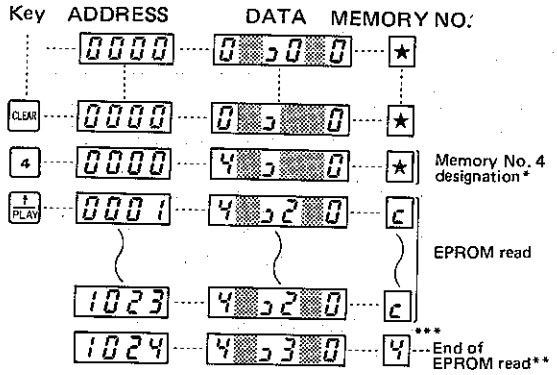
5.4 EPROM Read Operation

This operation is to transfer the contents of the specified EPROM memory (Nos. 1 thru 4) to the RAM.

- **Operating procedure**



- **Display**

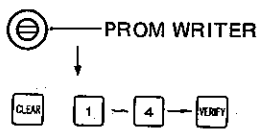


NOTES:
1. * One of memory Nos. 1 ~ 4 must be specified.
2. During the EPROM Read operation, if the power is turned off or the EPROM chip is removed, the EPROM read will be interrupted. In such a case, retry the operation from the beginning.
3. ** When the EPROM Read operation is completed or when an error occurs during the EPROM Read operation, the buzzer issues intermittent beep sounds to alert the operator.
4. Be sure to perform the EPROM Verify operation to check if the data have been read properly by the RAM.
5. *** Upon completion of the EPROM Read operation, the specified memory No. will be indicated on the MEMORY No. display.
6. Approx. 4 minutes are required to complete one EPROM Read operation.

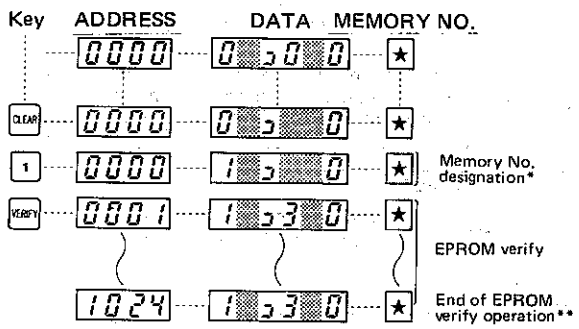
5.5 EPROM Verify Operation

This operation is to verify the contents of the specified EPROM memory (Nos. 1 thru 4) against the contents of the RAM.

- **Operating procedure**



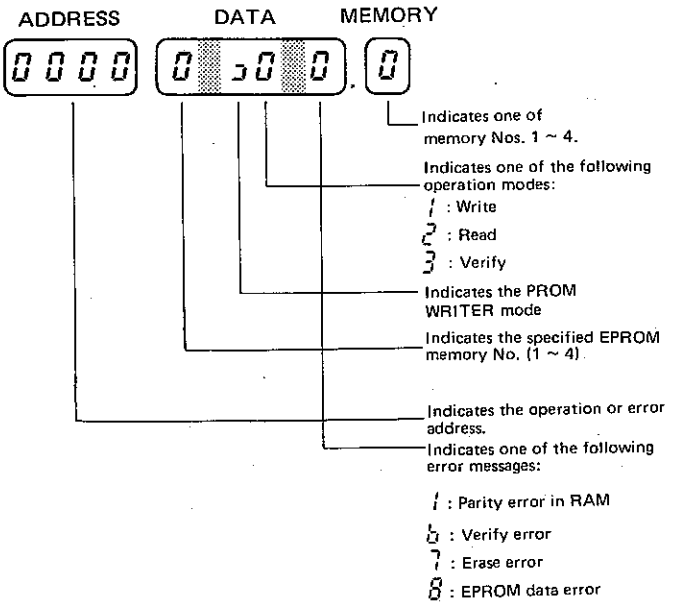
- **Display**



NOTES:
1. * One of memory Nos. 1 ~ 4 must be specified.
2. During the EPROM Verify operation, if the power is turned off, or the EPROM chip is removed, the EPROM Verify operation will be interrupted. In such a case, retry the operation from the beginning.
3. ** Upon completion of the EPROM Verify operation, the buzzer issues intermittent beep sounds to alert the operator.

5.6 Error in PROM WRITER Mode

During an EPROM Write, Read or Verify operation, the following indications may appear on the ADDRESS, DATA and MEMORY No. displays respectively.

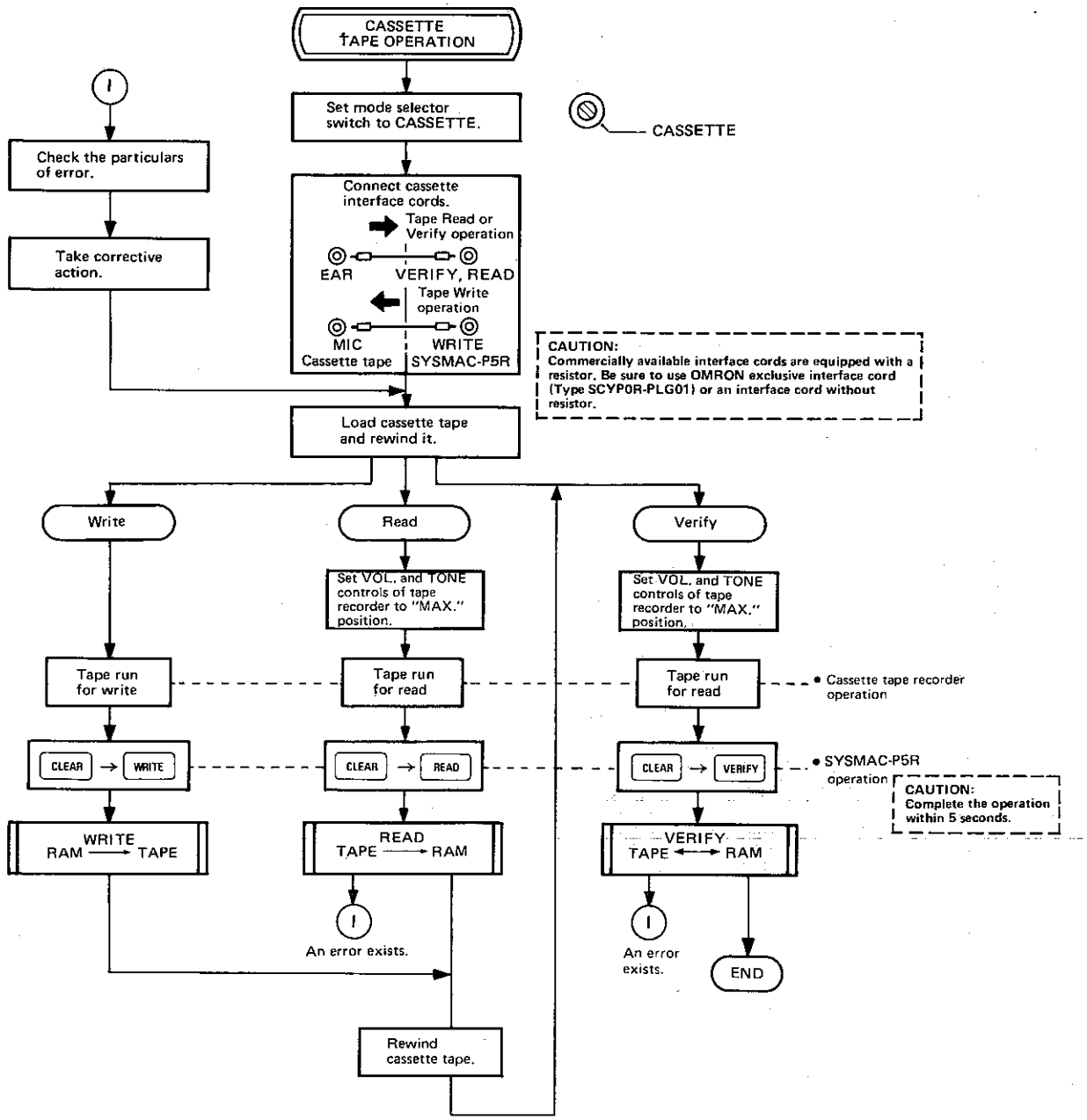


The description of each error message is as follows.

Operation	Error	Description of message
EPROM Write	1	A parity error has occured in the RAM.
	7	No. 1 EPROM memory has not been erased.
EPROM Verify	1	A parity error has occurred in the RAM.
	6	The contents of the specified EPROM memory No. (1 ~ 4) do not coincide with those of the RAM.
EPROM Read	8	No data exists in the specified EPROM memory No. (1 ~ 4)

5.7 Cassette Tape Handling

As a method of keeping user programs in storage, data may be recorded on a cassette tape by using a commercially available cassette tape recorder.
In the following, a general operational flowchart is shown.



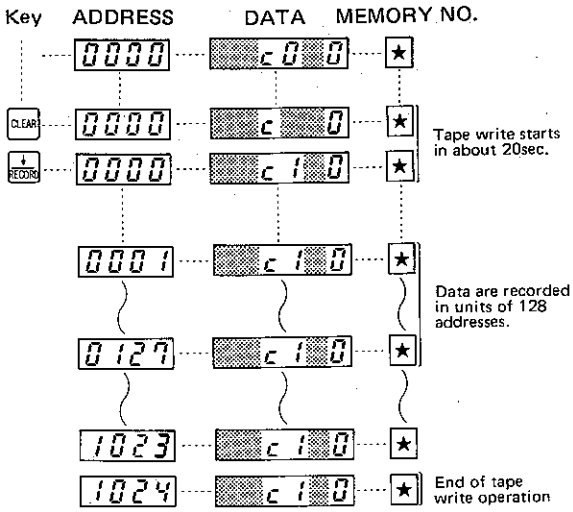
NOTES:
1. Be sure to use a monaural cassette tape recorder.
2. Use a new battery for the cassette tape recorder.
3. Always use a new cassette tape for recording. Note that the presence of scratches or other damage on the tape surface prevents data from being written or read properly.
4. Voltage drop of the battery in the cassette tape recorder results in a decrease in the output level and consequently a failure in signal discrimination.

5.8 Tape Write Operation

This operation is to record the contents of the RAM (program memory) on a cassette tape.

- **Operating procedure**
  Refer to 5.7, Cassette Tape Handling.

- **Display**



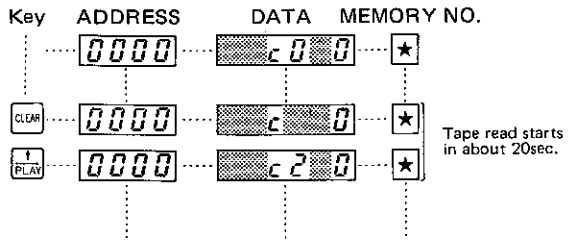
NOTES:
1. Upon completion of the Tape Write operation, be sure to perform the Tape Verify operation to confirm that the data have been recorded on the tape properly.
2. Error detection cannot be performed during the Tape Write operation. Even if the tape does not run, data will be transferred unilaterally from the RAM. So, be sure to confirm that the tape is running smoothly.
3. If the power is turned off or the cassette is ejected during the Tape Write operation, the tape write will be interrupted. Retry the tape write operation from the beginning.
4. During the Tape Write operation, no PROGRAM key input will be accepted.
5. For the Tape Write operation, use the WRITE → MIC jack to connect one of the cassette tape interface cords. For subsequent verify operation, use VERIFY READ ← EAR jack.
6. Approx. 6 minutes are required to complete one Tape Write operation.

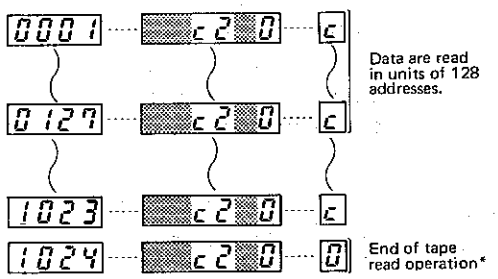
5.9 Tape Read Operation

This operation is to transfer the program data recorded on the cassette tape into the RAM.

- **Operating procedure**
  Refer to 5.7, Cassette Tape Handling.

- **Display**





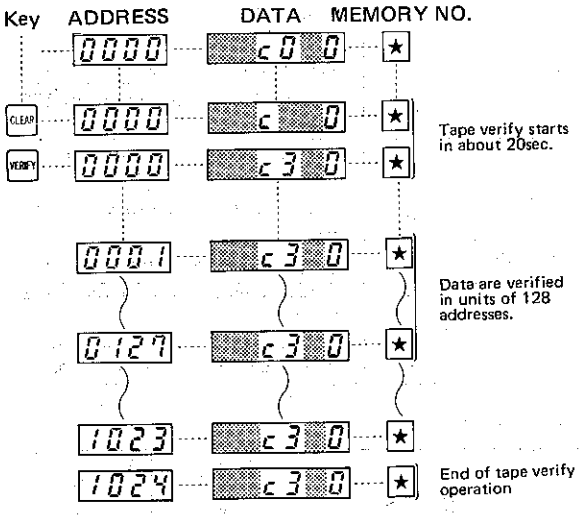
NOTES:
1. Upon completion of the Tape Read operation, be sure to perform the Tape Verify operation to confirm that the data have been transferred properly from the tape to the RAM.
2. If the power is turned off or the cassette is ejected during the Tape Read operation, the tape read will be interrupted. Retry the tape read operation from the beginning.
3. During the Tape Read operation, no PROGRAM key input will be accepted.
4. Be sure to set the volume control and tone control of the cassette tape recorder to maximum.
5. * Upon completion of the Tape Read operation, the MEMORY No. display will indicate "0."
6. Approx. 6 minutes are required to complete one Tape Read operation.

5.10 Tape Verify Operation

This operation is to verify the contents of the RAM against the programmed data recorded on a cassette tape.

- **Operating procedure**
  Refer to 5.7 Cassette Tape Handling.

- **Display**

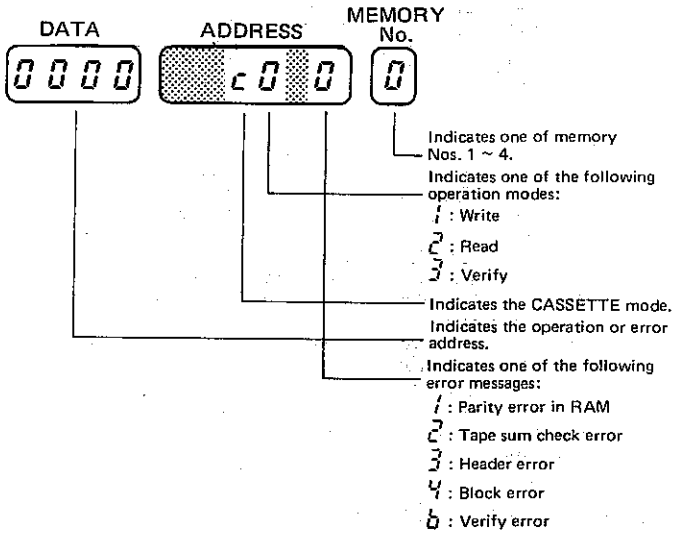


NOTES:
1. If the power is turned off or the cassette tape is ejected during the Tape Verify operation, the tape read will be interrupted. Retry the tape verify operation from the beginning.
2. During the Tape Verify operation, no PROGRAM key input will be accepted.
3. Be sure to set the volume control and tone control of the cassette tape recorder to maximum.

5.11 Errors in Cassette Mode

During Tape Write, Read, or Verify operation, the following indications may appear on the ADDRESS, DATA and MEMORY No. display respectively.

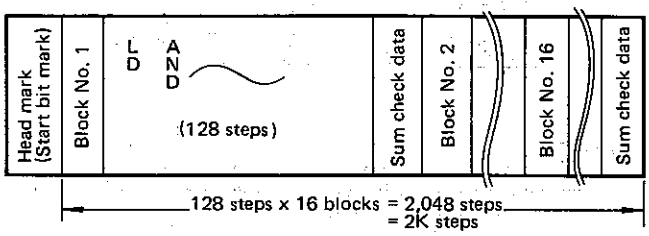
- **Display**



The description of each error message is shown below.

Operation	Error message	Description of message
Tape write	1	A parity error has occurred in the RAM.
Tape read	2	A sum check error exists in the tape data.
	3	A start bit error in units of 128 steps.
	4	A record No. error in units of 128 steps.
Tape verify	1	A parity error has occurred in the RAM.
	2	A sum check error exists in the tape data.
	3	A start bit error in units of 128 steps.
	4	A record No. error in units of 128 steps.
	5	The contents of the RAM do not coincide with those of the tape.

- **Tape format**



5.12 Cautions in Operating SYSMAC-P5R

When operating the SYSMAC-P5R, pay attention to the following points.

CAUTIONS:

- **Before connecting the CPU with the I/O unit, be sure to turn off the AC power being supplied to the SYSMAC-P5R.**
- **Before power application, be sure to set the desired supply voltage using the voltage selector switch. (The rated voltage is factory-set to AC 240V prior to shipment.)**
- **The key inserted into the mode selector switch can be removed at either the RUN or MONITOR position. However, when the key inserted into the mode selector switch is removed at the MONITOR position, the SYSMAC-P5R is capable of performing such operations as search, monitor, trace check, etc.**

6. Installation and Wiring

The SYSMAC-P5R is a highly reliable programmable controller which is resistant to adverse environmental conditions. However, in order to permit the programmable controller to fully exhibit its functions, as well as to enhance its reliability, care must be exercised on the following points when installing the programmable controller.

6.1 Mounting Locations and Environmental Conditions

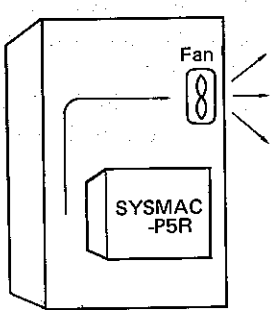
When installing the SYSMAC-P5R programmable controller, avoid the following locations.

- Location where the ambient temperature is beyond the range of 0 to 50°C.
- Location where temperature changes abruptly, thus resulting in condensation.
- Location where relative humidity exceeds the range of 30 to 90%.
- Location subject to corrosive gas or flammable gas.
- Location subject to excessive dust, salt, or iron particles.
- Location subject to vibration or shock.
- Location subject to direct sunlight.

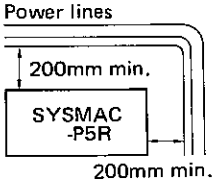
6.2 Mounting Positions within Control Panels

When mounting the SYSMAC-P5R in a control panel, take into consideration the operability, maintenability and environmental resistance of the programmable controller.

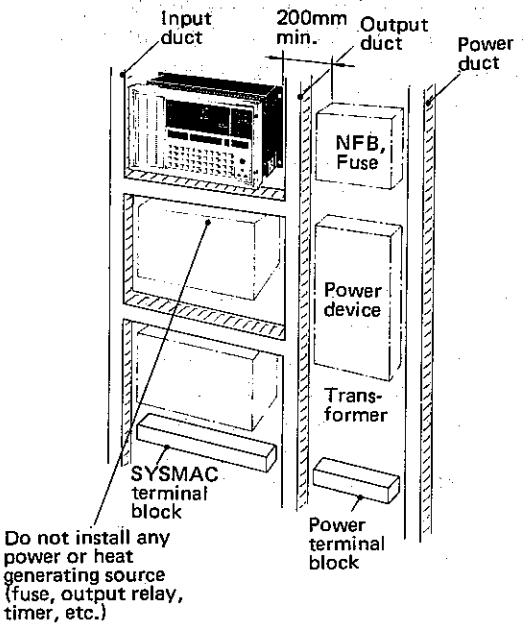
1. To permit the use of the SYSMAC-P5R within the ambient operating temperature range, pay attention to the following points.
   a. Provide the programmable controller with adequate space for ventilation.
   b. Avoid mounting the controller directly above any heat generating sources (heater, transformer, resistor of high capacity).
   c. Install a fan for forced ventilation if the ambient temperature exceeds 50°C.



2. Avoid mounting the SYSMAC-P5R in a panel in which high-tension equipment is installed.
3. Provide a distance of more than 200mm between the high-tension or power lines and the SYSMAC-P5R.



4. Mount the SYSMAC-P5R as far away as possible from high-tension equipment or power devices for the sake of safety in maintenance and operation.

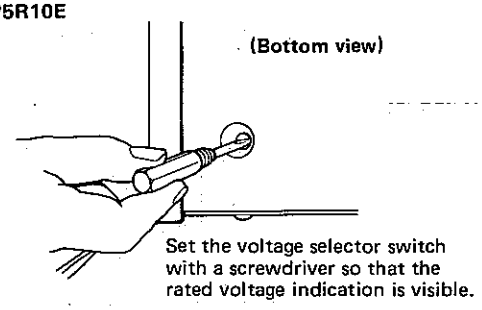


5. Mounting the SYSMAC-P5R at a height 1,000 to 1,600mm above the installed surface of the control panel will facilitate the operation of the programmable controller.

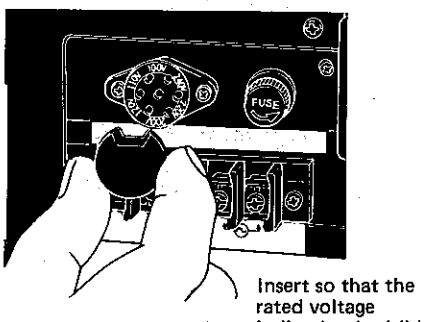
6.3 Processing of Wiring within Control Panel

1. Power supply and wiring
   - Before power application, be sure to set the desired supply voltage using the voltage selector switch at the bottom of the I/O unit. (The rated voltage is factory-set to AC 240V prior to shipment.)

SCY-P5R10E

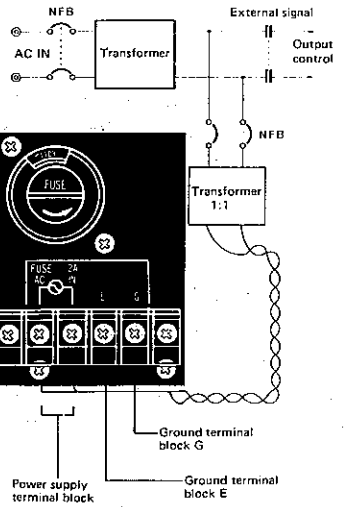


SCY-P5R30E

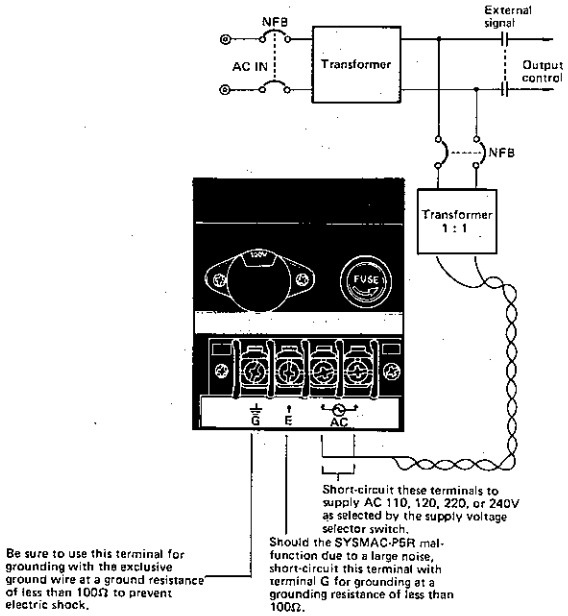


- As the power supply line of the SYSMAC-P5R, employ a wire of 2mm^2 min. so as to prevent voltage drop. (Use of twisted pair wires is recommended.)
- For general noise on the power supply line, the noise suppressing circuit in the SYSMAC-P5R is sufficient. However, supplying power through a transformer having a transformer voltage ratio of 1:1 will help reduce equipment-to-ground noise to a great extent and installation of such a transformer is recommended. Terminal G of the I/O unit is a ground terminal used for prevention of electric shock. Use an exclusive ground wire (having a conductor cross-sectional area of 2mm^2 min.) for grounding at a grounding resistance of less than 100Ω.
  Terminal E is a noise filter neutral terminal and the grounding is not basically required. In case of a large noise which may cause an erroneous operation, E and G are short-circuited for exclusive grounding (at a grounding resistance of less than 100Ω.)

- **SCY-P5R10E**



- **SCY-P5R30E**



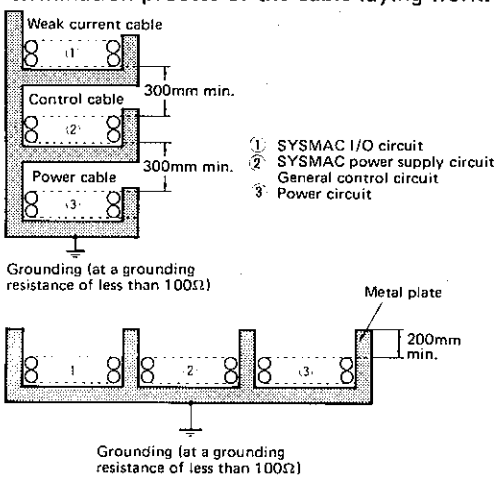
Note that common use of the grounding line with other equipment or connecting to the beam of the building may adversely affect the system.
Keep the length of the ground wire within 20m.
Care must be taken to the grounding resistance as it varies depending on the nature of ground, water content, seasons and the time elapsed after the underground laying of the ground wire.

6.4 Operation at Power Failure

1. As the power supply of the SYSMAC-P5R, supply power within +10%, −15% of the supply voltage.
2. The power sequence circuit is incorporated in the power supply unit of the SYSMAC-P5R to prevent the programmable controller from malfunctioning due to a momentary power failure or a decrease in the supply voltage.
   a. Supply voltage drop
      If the supply voltage drops below its 85%, the alarm buzzer sounds and the operation of the SYSMAC-P5R stops, causing external output relays to turn off.
   b. Momentary power failure
      If a momentary power failure of more than 1 cycle or a voltage drop to less than 85% of the supply voltage occurs, the power failure detecting circuit of the SYSMAC-P5R functions to stop the programmable controller automatically.
   c. Automatic reset
      The SYSMAC-P5R will automatically resume its operation after the supply voltage (more than 85%) is restored.

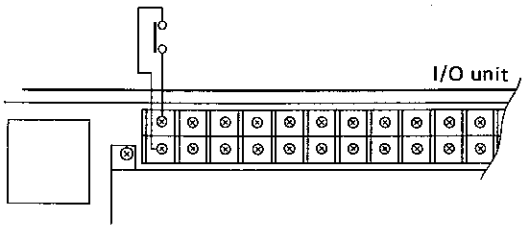
6.5 External Wiring

1. Be sure to process the input/output lines of the SYSMAC-P5R separately from other control lines. (Do not share the conductors of the I/O cable with others.)
2. To process the cables for the SYSMAC-P5R with power cables rated at 400V 10A max. or 220V 20A max.:
   a. Be sure to provide a minimum distance of 300mm between both cables when their racks are paralleled.
   b. Be sure to screen them with grounded metal plate when both cables are placed in the same duct at the termination process of the cable laying work.

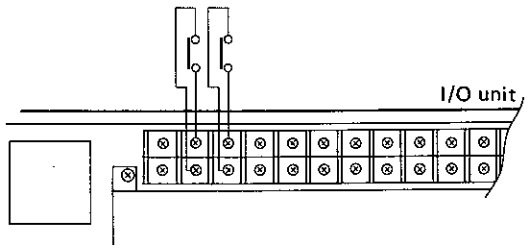


6.6 Hints on Use of Control I/O Relay

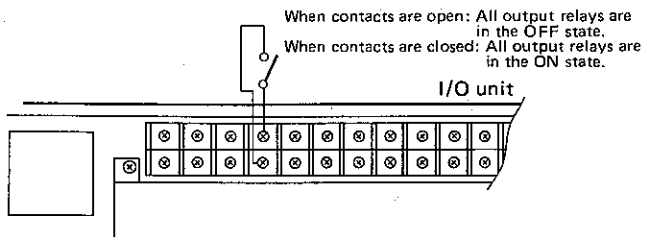
- **Memory/CPU failure output**
  This output is a no-voltage contact (SPST-NO) output which is activated (ON) when a memory or CPU failure occurs while the CPU is in the RUN or MONITOR mode.

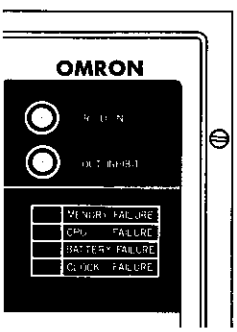


- **RUN output**
  This output is a non-voltage contact (DPST-NO) output which is activated (ON) while the CPU is in the RUN mode. The output, however, is inactivated (OFF) whenever a memory or CPU failure occurs.

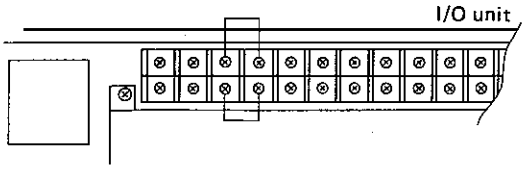


- **OUTPUT INHIBIT input**
  When the OUT INHIBIT input terminals are short-circuited (i.e., closed), the output relays operate and when the input terminals are disconnected (i.e., open), the output relays release, and the OUT INHIBIT indicator is illuminated. If the OUTPUT INHIBIT input is not required, leave the input terminals in the short-circuited state at all times by connecting them with a lead wire. (In other words, the output relays will not operate unless the OUT INHIBIT input terminals are short-circuited.)





When a CPU failure occurs, all the output relays will also release. However, in the event of a memory failure (parity error), the output state of each relay at the time of the failure is retained. By connecting terminals as shown below, the output relays can be set to release when a memory or CPU failure occurs and to operate while the CPU is in the RUN mode.

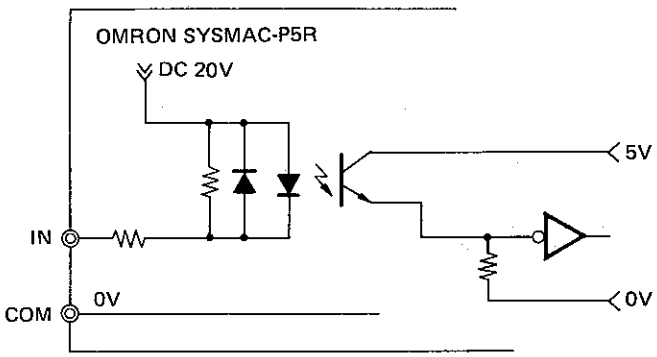


6.7 Output Forms of Input Switches and Methods of Interfacing SYSMAC-P5R

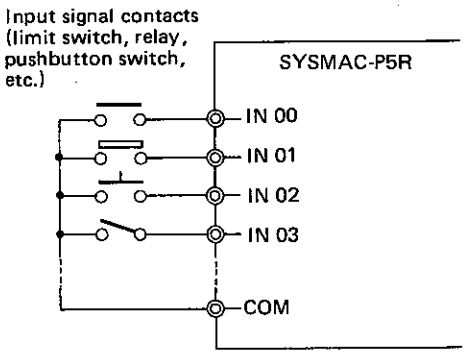
- **Input system: Sink type**
  1. Input characteristics

Input voltage:	DC 20V (unregulated power supply)	
Input current:	10mA TYP.	
Input impedance:	1.6kΩ	
Input threshold level:	[ON]	5mA min.
	[OFF]	2mA max.

  2. Input circuit diagram

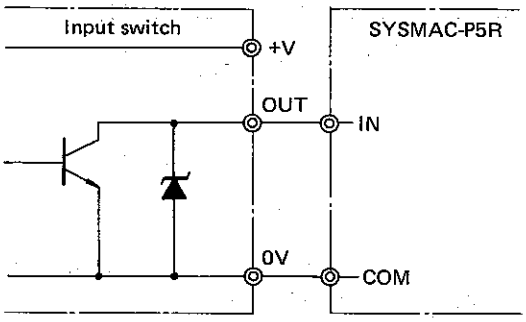


- **In case of contact input:**
  When a contact (no-voltage contact) input is employed, connect one of the input lines to the COM terminal and the others to the IN terminals (00 to 47).

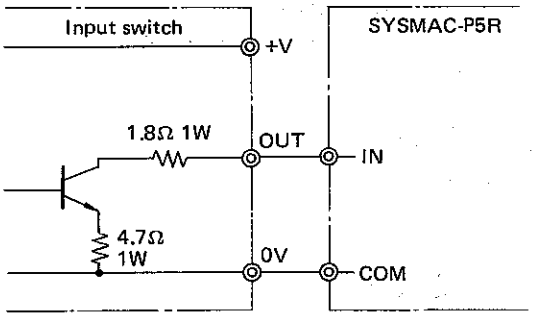


- **In case of solid-state input:**
  When using solid-state input switches, pay attention to the output forms of the respective input switches. The following are examples interfacing with OMRON proximity switches and photoelectric switches.

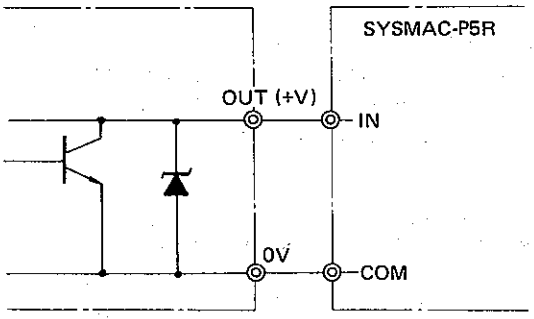
1. NPN open collector type:
   This type can be used.



Applicable models
- OMRON proximity switches
  Type TL-XP□(M) series
  (+V: DC 10 to 30V)
  Type E2M-□P□ series
  (+V: DC 24V)

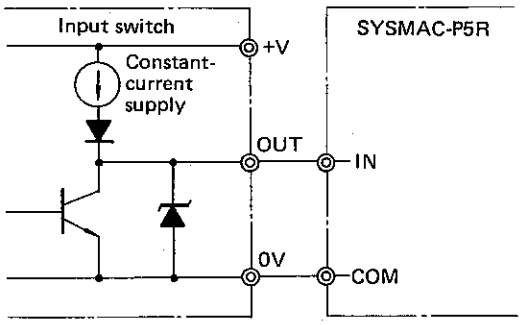


Applicable models
- OMRON proximity switches
  Type TL-LP50
  (+V: DC 10 to 30V)



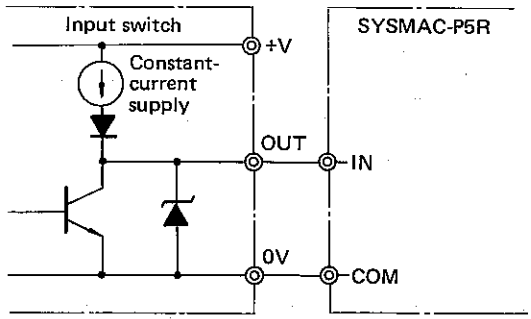
Applicable models
- OMRON proximity switches
  Model TL-XD
  (+V: DC 8 to 40V)

2. NPN output type:
   This type can be used.



Applicable models
- OMRON proximity switches
  Type TL-X□E□ series
  (+V: DC 10 to 40V)

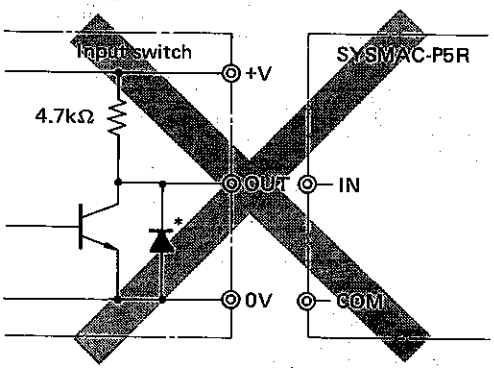
This type can be used conditionally.



Condition of use: DC 40V $\geq$ +V $\geq$ DC 24V

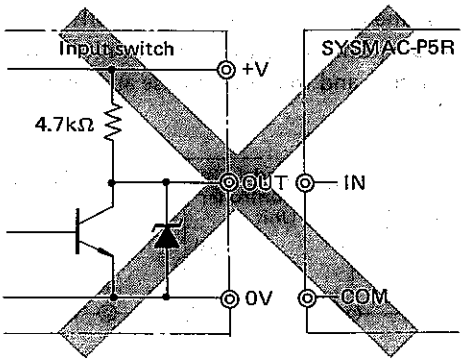
Applicable models
- OMRON photoelectric switches
  Model E3S series
  Model E3S-L series
  Model E3S-G series
  Model E3S-X series
  Model E3N series
  (+V: DC 12 to 24V)

This type cannot be used.

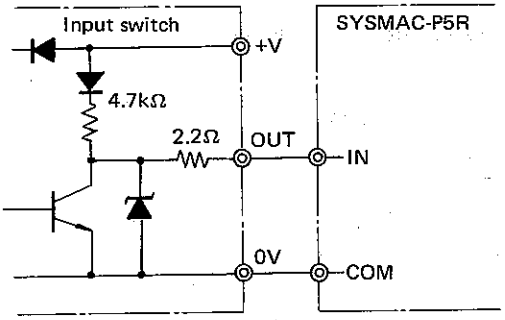


Models not applicable
- OMRON proximity switches
  Type TL-X□(M) series
  (+V: DC 10 to 14V)
  Type TL-N□/-H□/-F□ series
  (+V: DC 12V)
  Type TL-G□/-Q□ series
  (+V: DC 12V)

NOTE: For Type TL-G□, the diode marked * is not provided, but a capacitor (0.01μF) is incorporated instead.



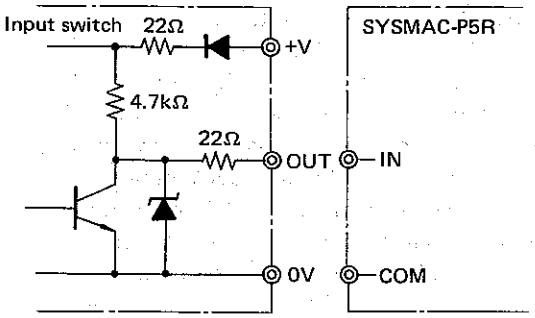
Models not applicable
- OMRON proximity switches
  Type E2M-□□ series
  (+V: DC 12V)



Condition of use: +V DC 24V ±20%

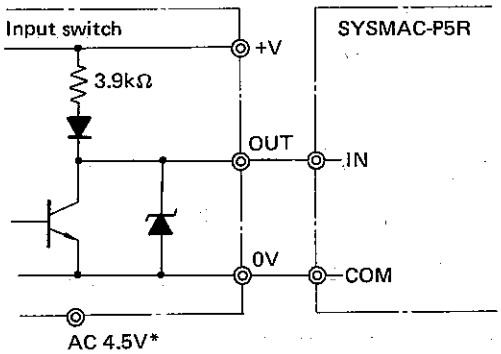
Applicable models
- OMRON proximity switches
  Type TL-M□E□ series
  (+V: DC 10 to 30V)

This type can be used conditionally.



Condition of use: +V DC 24V ±20%

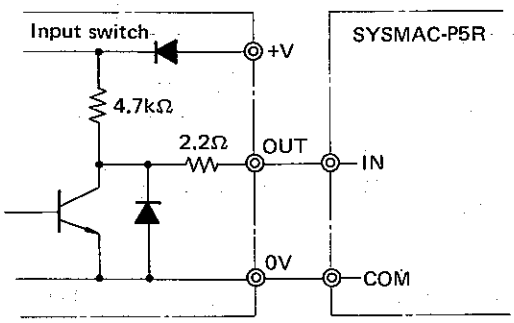
Applicable models
- OMRON proximity switches
  Type E2K-C25ME□ series
  (+V: DC 10 to 40V)



Condition of use: +V DC 24V ±20%

Applicable models
- OMRON photoelectric switches
  Type E3ML-□E4-G series
  (+V: DC 10 to 30V)

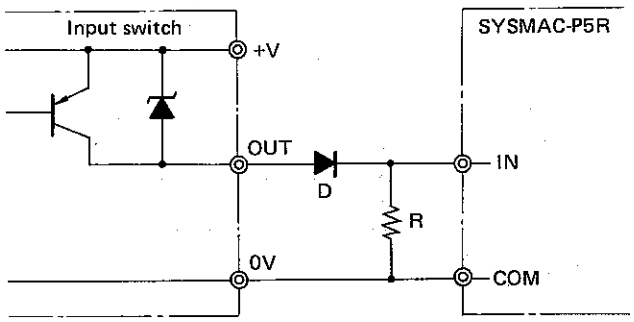
NOTE: * Power source for AC 4.5V lamp is necessary.



Condition of use: +V DC 24V ±20%

Applicable models
- OMRON proximity switches
  Type TL-N(F,H)□ME□ series
  (+V: DC 10 to 30V)

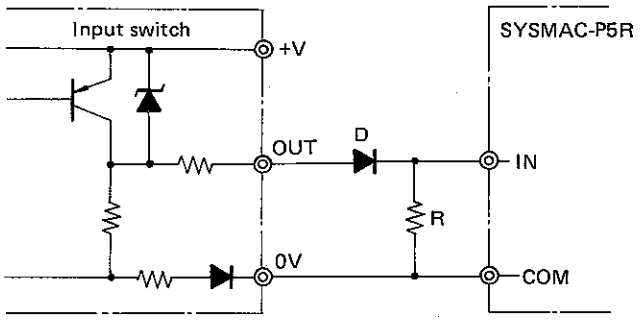
3. PNP open collector type:
   This type can be used conditionally.



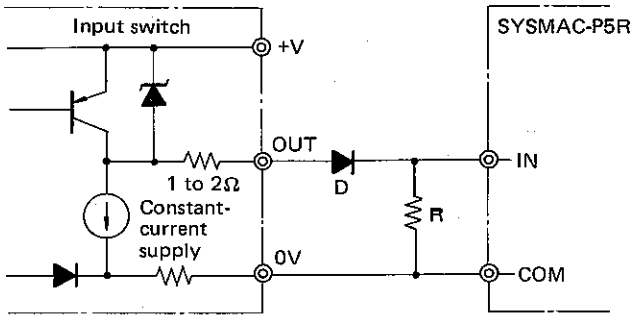
Condition of use: D: Capacity must be 30mA min.
R: 1kΩ, 2W
DC 40V ≧ +V ≧ DC 24V

Applicable models
- OMRON proximity switches
  Type TL-XP□P(M) series
  (+V: DC 10 to 30V)

4. PNP output type:
This type can be used conditionally.

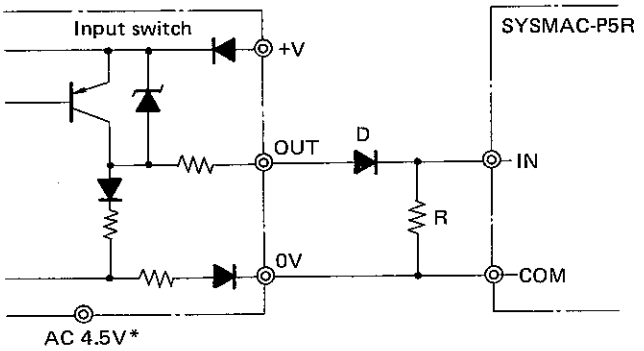


Applicable models
- OMRON proximity switches
  Type E2K-C25MF□ series
  (+V: DC 10 to 40V)



Condition of use: D: Capacity must be 30mA min.
R: 1kΩ, 2W
DC 40V ≥ +V ≥ DC 24V

Applicable models
- OMRON proximity siwtches
  Type TL-X□F□ series
  (+V: DC 10 to 40V)



Condition of use: D: Capacity must be 30mA min.
R: 1kΩ, 2W
DC 30V ≥ +V ≥ DC 24V

Applicable models
- OMRON photoelectric switches
  Type E3ML-□F4-G series
  (+V: DC 10 to 30V)
  NOTE: * Power source for AC 4.5V lamp is necessary.

For the methods of interfacing described in the types that can be used conditionally, if difficult to use, and in the types that cannot be used, interface the SYSMAC-P5R with the solid-state input switches through contact input as follows.

One way is to use the contact output of the OMRON Model S3S controller unit for OMRON proximity and photoelectric switches and the other to use an electromagnetic relay.

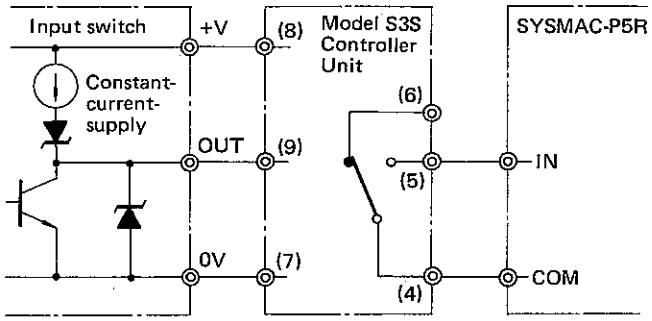
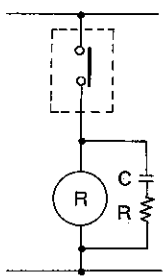


Figure in parentheses denotes terminal No.

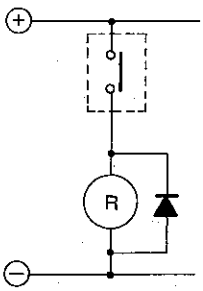
6.8 Hints on Use of Output Contacts

- If any electrical devices, which are likely to generate electric noise, are to be employed as the output loads of the SYSMAC-P5R, be sure to take measures to absorb such noise. For example, electromagnetic relays, valves, etc. generating a noise of 1,200 to 1,300V minimum are subject to noise suppression. For AC operated noise sources, connect a surge suppressor in parallel with the coil of each device. For DC operated noise sources, connect a diode in parallel with the coil of each device.



AC power source

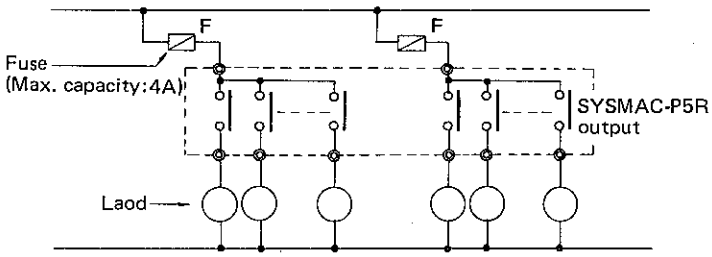
C: 0.5μF ±20% min.
Nonpolarity
Withstand voltage: 1,500V min.
R: 50Ω ±30%, 0.5W



DC power source

Select a diode with the breakdown voltage and current ratings according to the load.

- Since the output contacts (SPST-NO) of the SYSMAC-P5R consist of relay contacts which are packaged on a printed circuit board and connected to the terminal board, short-circuiting any of loads connected to the output contacts may result in the burning of, and consequent damage to, the P.C. board. Therefore, use of fuses is recommended for protection of the output contacts.



7. Maintenance and Inspection

To sustain the proper system operation at all times, it is necessary to inspect the SYSMAC-P5R daily. If any trouble occurs in the SYSMAC-P5R, how the system should be protected and how soon it can be recovered from the failure become important. In this chapter, the items to be inspected on the SYSMAC-P5R and the actions to be taken if the SYSMAC-P5R fails are described.

7.1 Inspection

To make the most of the functions of the SYSMAC-P5R under the best condition, it is necessary to inspect the SYSMAC-P5R daily or periodically.

■ INSPECTION ITEMS

The SYSMAC-P5R employs semi-conductors as its main component elements and has few or no supplies with a limited service life. However, the semi-conductors may deteriorate depending on the environmental conditions and must therefore be inspected periodically. The standard inspection cycle is 6 months to 1 year. According to the environmental conditions, it is recommended to advance the date of inspection. As a result of the daily or periodical inspection, if the SYSMAC-P5R is found to be outside the criteria in the following table, be sure to correct the SYSMAC-P5R so that it falls within the prescribed criteria.

No.	Inspection item	Particulars of inspection	Criteria
1	AC power supply (a) Voltage (b) Fluctuation	(1) Is the rated voltage available when measured within the I/O unit and at the AC input terminal block?	AC 110, 120, 220, or 240V +10%, −15%
		(2) Does a momentary power failure occur frequently or is there any sharp rise or drop in the supply voltage?	The supply voltage must be within the permissible fluctuation range described above.
2	Environmental conditions (a) Ambient temperature (b) Humidity (c) Vibration (d) Dust, etc.	Are the temperature and humidity within the respective range? (When the SYSMAC-P5R is installed in a control panel, the temperature within the panel may be regarded as the ambient temperature of the programmable controller.)	(a) 0 to +50°C (b) 30 to 90% RH (c) Must be free from vibration (d) Must be free from dust
3	Mounting conditions	(1) Are the I/O unit and CPU secured firmly?	The mounting screws must not be loose.
		(2) Are the connectors for the connecting cables of the I/O unit inserted completely?	The connecting cables must not be loose.
		(3) Is there any loose screw in the external wiring?	The screw terminals must not be loose.
		(4) Is there any broken cable in the external wiring?	The external wiring must be free from any abnormalities in apppearance.
4	Service life	(1) Output relays in the I/O output	Replace with new ones if defective.
		(2) Battery	1 year

CAUTION:
Be sure to turn off the power before replacing any unit (CPU or I/O unit) of the SYSMAC-P5R.

■ NOTES ON INSPECTION

1. If a defective unit is discovered and replaced, confirm whether or not the replaced unit is abnormal.
2. In the event of a faulty contact of the cable, wipe the connector pins with a clean all-cotton cloth moistened with industrial alcohol. Be sure to plug in the flat cable after removing the cloth waste.

■ TOOLS AND TESTING EQUIPMENT REQUIRED FOR MAINTENANCE

In the maintenance of the SYSMAC-P5R, the following tools and testing equipment will facilitate the daily or periodic inspection of the programmable controller.

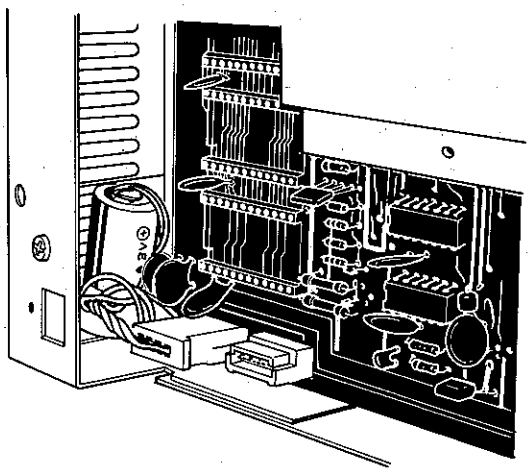
1. Tools and testing equipment recommended as mandatory equipment
   - Screwdrivers (Phillips and round blade)
   - Tester or digital voltmeter
   - Industrial alcohol and all-cotton cloth
2. Measuring instruments recommended only if required.
   - Synchroscope
   - Pen-recording oscilloscope

■ MAINTENANCE PARTS

1. I/O unit
   If the SYSMAC-P5R fails, its repair is impossible without any spare parts no matter how early the trouble is discovered. So, it is recommended to have at least one I/O unit as a spare part.
2. Battery (Type SCYP5R-BAT01)
   In general, the service life of a battery is regarded as the time when the capacity of the battery is reduced to 50% of its nominal capacity. The service life of a battery varies greatly depending on the ambient temperature of the battery, depth of discharging, discharge current, etc. With the SYSMAC-P5R, the life of the built-in battery is considered to be 1 year. Therefore, replace the battery with a new one every year.
3. AC power fuse: Rated at 3A

7.2 Replacement of Battery

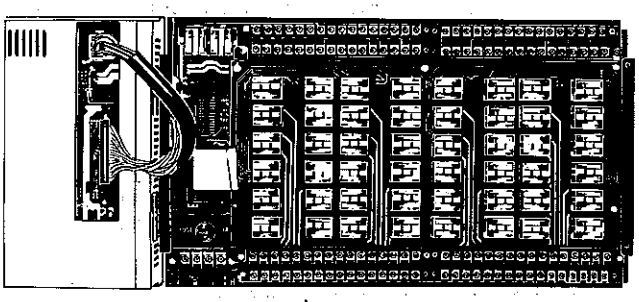
- **Procedure:**
  1. Prepare the replacement battery (Type SCYP5R-BAT01).
  2. Turn off the AC power.
  3. Remove the screw on the rear panel of the CPU and open the door as shown below.

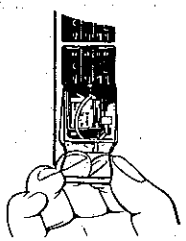


4. **Two battery connector sockets are provided. Plug the connector of the new battery into the vacant socket, and then unplug the connector of the old battery to remove it.**
5. Close the door, and secure it with the screw.
6. When the AC power is applied, the battery starts operating.

7.3 Replacement of Relays

- **I/O Unit in SCY-P5R10E**



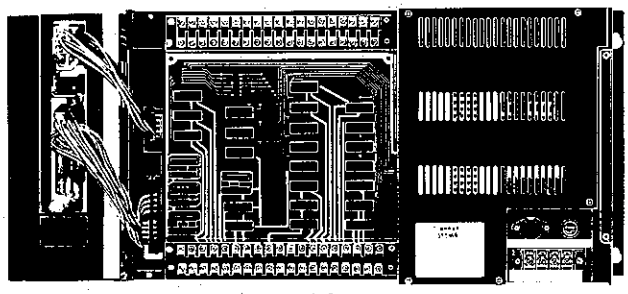


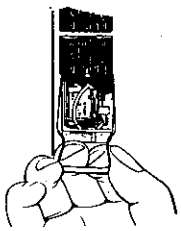
NOTES:
1. The SCY-P5R10E incorporates 48 OMRON Type MY2 (-US) relays rated at 24 VDC as output relays.
2. Output relays can be replaced easily by removing the I/O unit cover as shown above.
3. Be sure to use the same type of relays as replacement relays. Turn off the power supply when replacing output relays.
4. The OMRON Type MY2 relay is interchangeable with the OMRON Type G3F-203S solid-state relay. When the solid-state relays are desired as output relays due to the requirement to switch loads at high frequency, use the Type G3F-203S relays in place of the Type MY2 relays. The output specifications of the Type G3F-203S relays are as follows:

Max. permissible load	75 to 250 VAC 2A
Operate and release times	Zero cross applied
Leakage current	5mA max. (at 100 VAC) 10mA max. (at 200 VAC)

NOTE: Since one common terminal permits connection of 3 output points, be sure to limit the current flowing through each common terminal to less than 4A.

- **I/O Unit in SCY-P5R30E**





NOTES:
1. The SCY-P5R30E incorporates 24 output relays as follows.
   - Relay Nos. 50 ~ 69: OMRON Model G2L relays rated at 24 VDC
   - Relay Nos. 70 ~ 73: OMRON Type MY2 relays rated at 24 VDC
2. Only the Type MY2 relays can be replaced. Replacement of these relays can be performed easily by removing the I/O unit cover as shown above.
3. Be sure to use the same type of relays as replacement relays.
4. The OMRON Type MY2 relay is interchangeable with the OMRON Type G3F-203S solid-state relay. When the solid-state relays are desired as output relays due to the requirement to switch loads at high frequency, use the Type G3F-203S relays in place of the Type MY2 relays. In this case, however, only the output terminal numbers 70, 71, 72 and 73 are applicable.
   The output specifications of the Type G3F-203 relays are as follows:

Max. permissible load	75 to 250 VAC 2A
Operate and release times	Zero cross applied
Leakage current	5mA max. (at 100 VAC) 10mA max. (at 200 VAC)

NOTE: Since one common terminal permits connection of 3 output points, be sure to limit the current flowing through the common terminal to less than 4A.

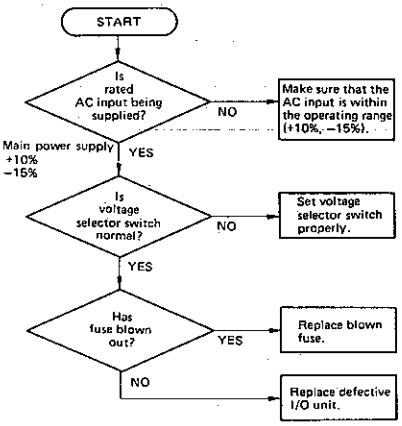
7.4 Troubleshooting

If any abnormality occurs in the SYSMAC-P5R, thoroughly grasp the condition of trouble, check whether the symptom is reproducible or is caused through relationship with other equipment, and then follow the troubleshooting flowcharts shown below.

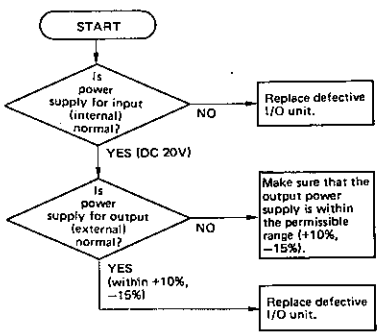
■ I/O UNIT

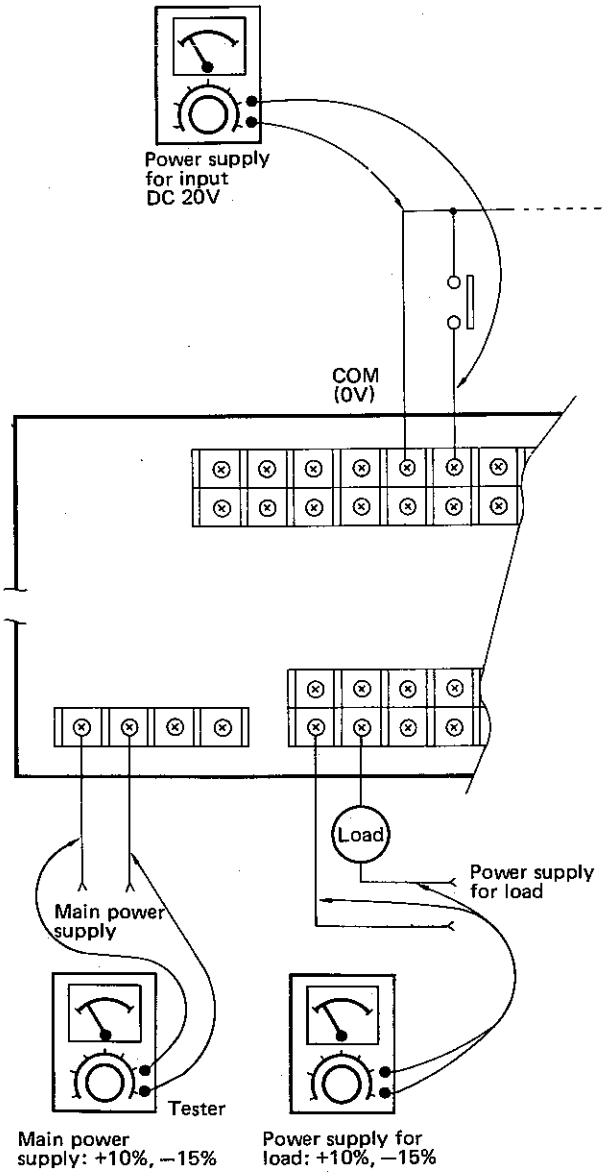
- **Main power supply check**

In this check, the AC power being supplied to the SYSMAC-P5R is confirmed if it is within the specified operating range.



- **I/O device related power supply check**

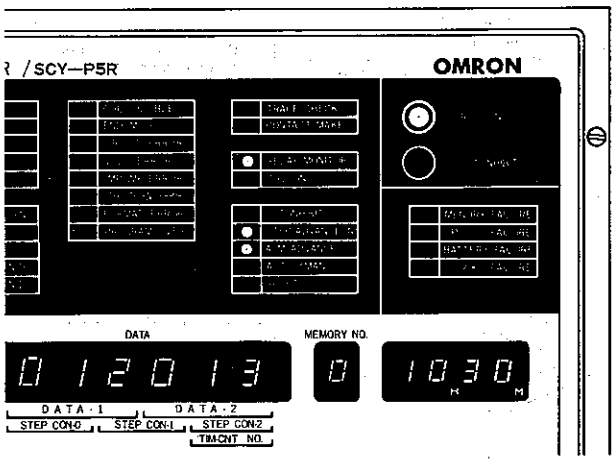


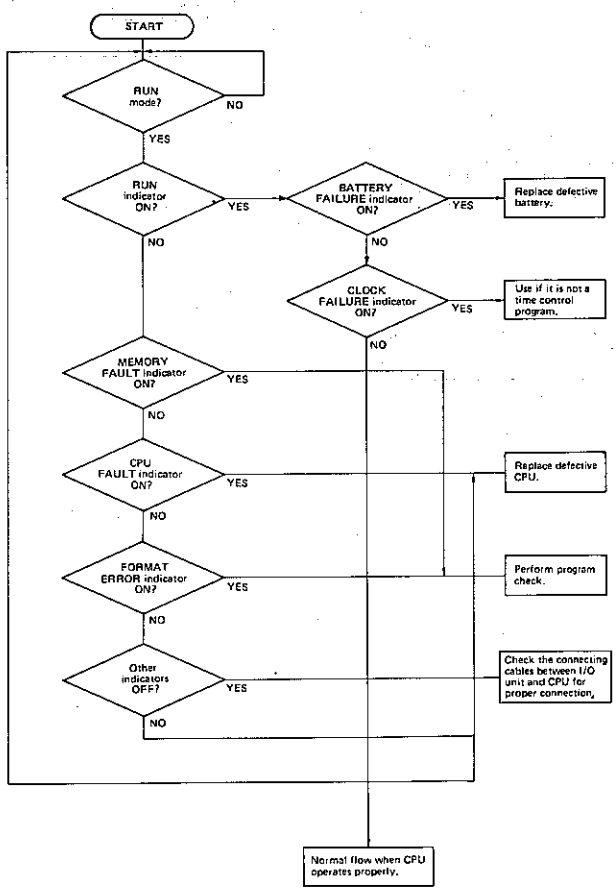


■ CPU

When the CPU is normally operating, the RUN indicator lights, the MEMORY No. display indicates 0 4, and the current time of day is displayed.

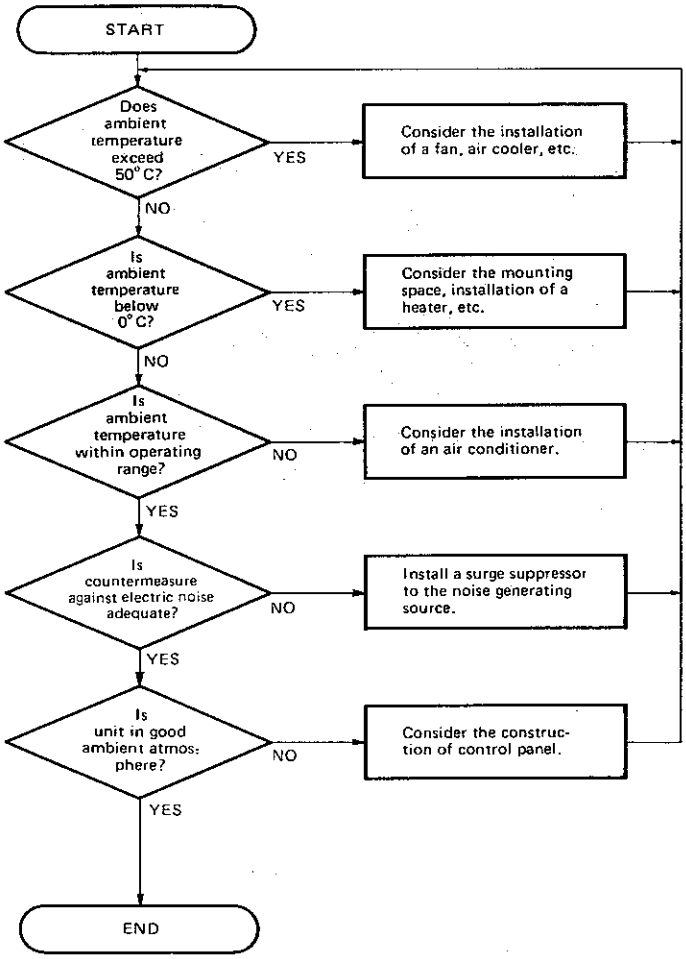
The following flowchart applies to the CPU if abnormality occurs in the unit while it is in the RUN mode.





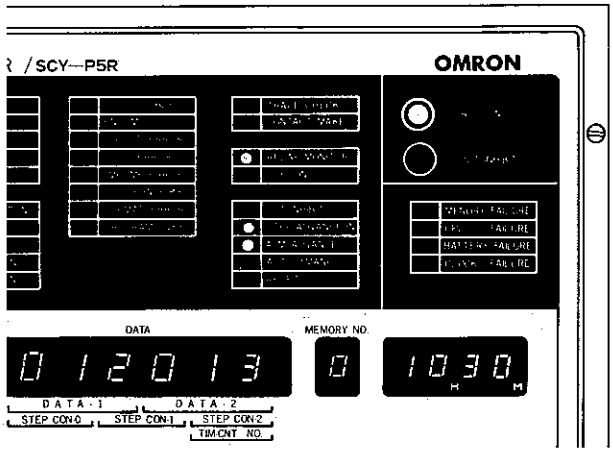
■ EXTERNAL ENVIRONMENTS

Confirm that the SYSMAC-P5R satisfies the environmental requirements described in Section 2.3, Specifications.



■ LIST OF ERROR MESSAGES

An error message appears in the DATA display as shown on the right.



Item / Mode	Symptom	Description of check/ condition of trouble	CPU fault output	Memory fault indicator	CPU fault indicator	Error message	Error indicator	Output relay	Remarks	Corrective action
RUN mode (MONITOR mode)	Memory failure	Parity check and format check	ON	●			●	Held as is.	CPU stops and control I/O relay operates at the same time.	Check and correct the program in PROGRAM mode.
	CPU failure	Watchdog timer check	ON		●		●	OFF		Turn the power off, then turn it on again.
	Battery failure	Rated voltage check					●	(235 ON)*	CPU continues to operate. The indicator illuminates while the time is being advanced.	Replace the battery with new one.
	Clock failure	24-hour clock check					●	(254 ON)*		Depress CLEAR key in MONITOR mode.
Program mode	No END instruction	Check the presence of END instruction at the end of a program.					●	OFF	The following key operation must be performed. CLEAR → SEARCH	Correct the program as necessary.
	Duplicate coil number	Check coil numbers for duplication.					●			
	Circuit error	Check the circuit for proper configuration.					●			
	IL-ILC error	Check INTERLOCK instructions for proper syntax.					●			
	JMP-JME error	Check JUMP instructions for proper syntax.					●			
	STEP-STEP END error	Check step advance type instructions for proper syntax.					●			
	Format error	Check each instruction for proper format.					●			
	Program over	Check memory capacity for overage.					●			
	CPU failure	Watchdog timer check	ON		●		●		These faults are independent of the user program.	Turn the power off, then turn it on again.
	Battery failure	Rated voltage check					●			Replace the battery with new one.
PROM WRITER mode	Parity error	Parity error check of RAM.		●		1	●	OFF	A memory number must be specified.	Perform program write in PROGRAM mode.
	Verify error	The contents of RAM do not coincide with those of EPROM.		○		6	○			Check the content of the program error.
	Erase error	EPROM erase check				7				Erase the EPROM chip again.
	Data error	No read data exists.				8				Insert the written EPROM chip into the socket.
	CPU failure	Watchdog timer check	ON		●		●		These faults are independent of the user program.	Turn the power off, then turn it on again.
	Battery failure	Rated voltage check					●			Replace the battery with new one.
Cassette mode	Parity error	Parity error check of RAM		●		1	●	OFF	The cassette tape operation must also be checked in conjunction with the CPU operation. (Refer to Chapter 5 for cassette tape handling.)	Perform program write operation again in PROGRAM mode.
	Sum error	Tape sum check				2				Perform Tape Read and Verify operations again. (Defective tape)
	Header error	Start bit error exists.				3				ditto
	Block error	Record No. error exists.				4				ditto
	Verify error	The contents of RAM do not coincide with those of the tape.		○		6	○			Check memory in PROGRAM mode.
	CPU failure	Watchdog timer check	ON		●		●		These faults are independent of the user program.	Turn the power off, then turn it on again.
	Battery failure	Rated voltage check					●			Replace the battery with new one.

NOTE: ● denotes that the indicator illuminates.
○ denotes that the indicator illuminates depending on the nature of failure or error.
* Special internal auxiliary relay.

I/O TERMINAL ASSIGNMENT TABLE FOR OMRON SYSMAC-P5R10E

Name		Model	Prepared by:	Inspected by:	Approved by:
Customer	Installation location	Drawing No. (Chip No.)			

00 ○ _____	16 ○ _____	32 ○ _____
01 ○ _____	17 ○ _____	33 ○ _____
02 ○ _____	18 ○ _____	34 ○ _____
03 ○ _____	19 ○ _____	35 ○ _____
04 ○ _____	20 ○ _____	36 ○ _____
05 ○ _____	21 ○ _____	37 ○ _____
06 ○ _____	22 ○ _____	38 ○ _____
07 ○ _____	23 ○ _____	39 ○ _____
08 ○ _____	24 ○ _____	40 ○ _____
09 ○ _____	25 ○ _____	41 ○ _____
10 ○ _____	26 ○ _____	42 ○ _____
11 ○ _____	27 ○ _____	43 ○ _____
12 ○ _____	28 ○ _____	44 ○ _____
13 ○ _____	29 ○ _____	45 ○ _____
14 ○ _____	30 ○ _____	46 ○ _____
15 ○ _____	31 ○ _____	47 ○ _____

50 ○ _____	66 ○ _____	82 ○ _____
51 ○ _____	67 ○ _____	83 ○ _____
52 ○ _____	68 ○ _____	84 ○ _____
53 ○ _____	69 ○ _____	85 ○ _____
54 ○ _____	70 ○ _____	86 ○ _____
55 ○ _____	71 ○ _____	87 ○ _____
56 ○ _____	72 ○ _____	88 ○ _____
57 ○ _____	73 ○ _____	89 ○ _____
58 ○ _____	74 ○ _____	90 ○ _____
59 ○ _____	75 ○ _____	91 ○ _____
60 ○ _____	76 ○ _____	92 ○ _____
61 ○ _____	77 ○ _____	93 ○ _____
62 ○ _____	78 ○ _____	94 ○ _____
63 ○ _____	79 ○ _____	95 ○ _____
64 ○ _____	80 ○ _____	96 ○ _____
65 ○ _____	81 ○ _____	97 ○ _____

I/O TERMINAL ASSIGNMENT TABLE FOR OMRON SYSMAC-P5R30E

Name		Model	Prepared by:	Inspected by:	Approved by:
Customer	Installation location	Drawing No. (Chip No.)			

00 ○	_____	16 ○	_____
01 ○	_____	17 ○	_____
02 ○	_____	18 ○	_____
03 ○	_____	19 ○	_____
04 ○	_____	20 ○	_____
05 ○	_____	21 ○	_____
06 ○	_____	22 ○	_____
07 ○	_____	23 ○	_____
08 ○	_____	24 ○	_____
09 ○	_____	25 ○	_____
10 ○	_____	26 ○	_____
11 ○	_____	27 ○	_____
12 ○	_____	28 ○	_____
13 ○	_____	29 ○	_____
14 ○	_____	30 ○	_____
15 ○	_____	31 ○	_____

50 ○	_____	66 ○	_____
51 ○	_____	67 ○	_____
52 ○	_____	68 ○	_____
53 ○	_____	69 ○	_____
54 ○	_____	70 ○	_____
55 ○	_____	71 ○	_____
56 ○	_____	72 ○	_____
57 ○	_____	73 ○	_____
58 ○	_____	74 ○	_____
59 ○	_____	75 ○	_____
60 ○	_____	76 ○	_____
61 ○	_____	77 ○	_____
62 ○	_____	78 ○	_____
63 ○	_____	79 ○	_____
64 ○	_____	80 ○	_____
65 ○	_____	81 ○	_____

OMRON SYSMAC-P5R CODING SHEET

Name		Model	Prepared by:	Inspected by:	Approved by:
Customer	Installation location	Drawing No. (Chip No.)			

Address	Step No.	OP	Data		STEP.CON Output setting															
			DATA-1	DATA-2																